

List of Publications

Atila Alvandpour, Professor

Electronic Devices Division
Department of Electrical Engineering
Linköping University

Journals:

- [1] A. Bhide, O. E. Najari, B. Mesgarzadeh, and A. Alvandpour, "An 8-GS/s 200-MHz Bandwidth 68-mW $\Delta\Sigma$ DAC in 65-nm CMOS", in IEEE Transactions on Circuits and Systems II, vol. 60, no. 7, pp. 387-391, July 2013.
- [2] Y. Jung; J. Fritzin, M. Enqvist, A. Alvandpour, "Least-Squares Phase Predistortion of a +30 dBm Class-D Outphasing RF PA in 65 nm CMOS", in IEEE Transactions on Circuits and Systems I, vol. 60, no. 7, pp. 1915-1928, July 2013.
- [3] Fazli Yeknami, F. Qazi and A. Alvandpour, "Low-Power DT $\Delta\Sigma$ Modulators Using SC Passive Filters in 65nm CMOS," in IEEE Transaction on Circuits and Systems-I, vol. pp, no. 99, pp. 1-13, 2013.
- [4] D. Svärd, C. Jansson and A. Alvandpour, "A Readout IC for an Uncooled Microbolometer infrared FPA with On-chip Self-heating Compensation in 0.35 μm CMOS", in Journal of Analog Integrated Circuits and Signal Processing, vol. 77, no. 1, pp. 29 - 44, Oct. 2013.
- [5] Fazli Yeknami and A. Alvandpour, "A 2.1 μW 80 dB SNR DT $\Delta\Sigma$ Modulator for Medical Implant Devices," in Journal of Analog Integrated Circuits and Signal Processing, vol. 77 , pp. 69-78, no. 1, Oct. 2013.
- [6] H. Raza Khan, J. Fritzin, A. Alvandpour , Q. Wahab," A parallel circuit differential class-E power amplifier using series", in Journal of Analog Integrated Circuits and Signal Processing, vol. 75, no. 1, pp. 31-40, April 2013.
- [7] P. Landin, J. Fritzin, W. Van Moer, M. Isaksson, and A. Alvandpour, "Modeling and Digital Predistortion of Class-D Outphasing RF Power Amplifiers," in IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 6, pp. 1907-1915, June 2012.
- [8] J. Fritzin, C. Svensson, and A. Alvandpour, "Analysis of a 5.5V Class-D stage used in +30 dBm outphasing RF PAs in 130nm and 65nm CMOS," in IEEE Transactions on Circuits and Systems-II, vol. 59, no.11, pp. 726-730, Nov. 2012.
- [9] J. Fritzin, C. Svensson, and A. Alvandpour, "Design and Analysis of a Class-D Stage with Harmonic Suppression," in IEEE Transactions on Circuits and Systems-I, vol. 59, no. 6, pp. 1178-1186, 2012.
- [10] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13- μm CMOS for Medical Implant Devices," in IEEE Journal of Solid-State Circuits, vol. 47, no. 7, pp.1585-1593, July 2012.
- [11] J. Fritzin, Y. Jung, P.N. Landin, P. Handel, M. Enqvist, and A. Alvandpour, "Phase Predistortion of a Class-D Outphasing RF Amplifier in 90nm CMOS," IEEE Transactions on Circuits and Systems-II, vol. 58, no. 10, pp. 642-646, Oct. 2011.

- [12] T. Sundström, C. Svensson, and A. Alvandpour, "A 2.4 GS/s, Single-Channel, 31.3 dB SNDR at Nyquist, 8-bit Pipeline ADC in 65nm CMOS," in *Journal of Solid State Circuits*, vol. 46, no. 7, pp. 1575-1584 July 2011.
- [13] J. Fritzin and A. Alvandpour, "A 3.3V 72.2Mbit/s 802.11n WLAN Transformer-Based Power Amplifier in 65nm CMOS" in *Journal of Analog Integrated Circuits and Signal Processing*, vol. 64, no. 3, pp. 241-247, Sept. 2010.
- [14] T. Sundström and A. Alvandpour, "A 6-bit 2.5-GS/s flash ADC using comparator redundancy for low power in 90 nm CMOS," in *Journal of Analog Integrated Circuits and Signal Processing*, vol. 64, no. 3, pp. 215 – 222, Sept. 2010.
- [15] T. Sundström and A. Alvandpour, "Utilizing Process Variations for Reference Generation in a Flash ADC", in *IEEE Trans. Circuits and Systems II*, vol. 56, no. 5, pp. 364- 368, May 2009.
- [16] B. Mesgarzadeh and A. Alvandpour, "A Low-Power Digital DLL-Based Clock Generator in Open-Loop Mode", in *IEEE Journal of Solid-State Circuits*, vol. 44, no. 7, pp. 1907-1913, 2009.
- [17] B. Mesgarzadeh, M. Hansson, and A. Alvandpour, "Jitter characteristic in charge recovery resonant clock distribution", in *IEEE Journal of Solid-State Circuits*, pp. 1618-1625, vol. 42, July 2007.
- [18] S. Vangal, Y. Hoskote, N. Borkar and A. Alvandpour, "A 6.2-GFlops floating-point multiply-accumulator with conditional normalization", in *IEEE Journal of Solid-State Circuits*, vol. 41, no. 10, pp. 2314-2323, Oct. 2006,
- [19] S. Hsu, A. Alvandpour, S. Mathew, S. Lu, R. Krishnamurthy, S. Borkar, "A 4.5GHz 130nm 32-kb L0 Cache with a Leakage-tolerant Self Reverse-Bias Bitline Scheme," *IEEE Journal of Solid-State Circuits*, vol.38, no.5, pp. 755-76, May 2003.
- [20] A. Alvandpour, R. Krishnamurthy, K. Soumyanath, S. Borkar, "A Sub-130nm Conditional Keeper Technique," *IEEE Journal of Solid-State Circuits*, vol. 37, no: 5, pp. 633-638, May 2002.
- [21] R. Krishnamurthy, A. Alvandpour, G. Balamurugan, N. Shanbhag, K. Soumyanath, S. Borkar, "A 130-nm 6GHz 256x32b Leakage-tolerant Register File," *IEEE Journal of Solid-State Circuits*, Vol.: 37, no: 5, pp. 624-63, May 2002.

International Conferences:

- [22] A. Ojani, B. Mesgarzadeh, and A. Alvandpour, "A Quadrature UWB Frequency Synthesizer with Dynamic Settling-Time Calibration", *IEEE Intl. Symp. Circuits and Systems (ISCAS)*, pp. 2480-2483, May 2013.
- [23] A. Fazli Yeknami, and A. Alvandpour, "A 0.5-V 250-nW 65-dB SNDR Passive $\Delta\Sigma$ Modulator for Medical Implant Devices", *IEEE Intl. Symp. Circuits and Systems (ISCAS)*, pp. 2010-2013, May 2013.
- [24] A. Fazli Yeknami, and A. Alvandpour, "A Variable Bandwidth Amplifier for a Dual-mode Low-Power $\Delta\Sigma$ Modulator in Cardiac Pacemaker System", *IEEE Intl. Symp. Circuits and Systems (ISCAS)*, pp. 1918-1921, May 2013.
- [25] D. Zhang and A. Alvandpour, "A 3-nW 9.1-ENOB SAR ADC at 0.7 V and 1 kS/s," in *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 369-372, September 2012.
- [26] B. Mesgarzadeh, I. Soderquist, and A. Alvandpour, "Reliability Challenges in Avionics due to Silicon Aging," in proc. *IEEE Intl. Symp. on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, pp. 342-347, April 2012.

- [27] A. Ojani, B. Mesgarzadeh, and A. Alvandpour, "A DLL-based Injection-Locked Frequency Synthesizer for WiMedia UWB," in proc. IEEE Symp. on Circuits and Systems (ISCAS), pp. 2027-2030, May 2012.
- [28] J. Fritzin, B. Mesgarzadeh, and A. Alvandpour, "A Class-D Stage with Third Harmonic Suppression and DLL Based Phase Generation," in proc. IEEE Midwest Symp. on Circuits and Systems (MWSCAS), pp. 45-48, August 2012.
- [29] A. Ojani, B. Mesgarzadeh, and A. Alvandpour, "A Process-Variation Tolerant DLL-Based UWB Frequency Synthesizer," in proc. IEEE Midwest Symp. on Circuits and Systems (MWSCAS), pp. 558-561, August 2012.
- [30] A. Fazli Yeknami and A. Alvandpour, "A 0.7-V 600-nW 87-dB SNDR DT- $\Delta\Sigma$ Modulator with Partly Body-Driven and Switched Op-amps for Biopotential Signal Acquisition," in Proc. IEEE Biomedical Circuits and Systems Conference (BioCAS), pp. 1-4, November 2012.
- [31] A. Fazli Yeknami and A. Alvandpour, "A 2.1 μ W 76 dB SNDR DT- $\Delta\Sigma$ Modulator for Medical Implant Devices," in Proc. IEEE Norchip, 12-13, pp. 1-4, November 2012.
- [32] D. Svard, C. Jansson, and A. Alvandpour, "A Readout Circuit for an Uncooled IR Camera With Mismatch and Self-Heating Compensation," in IEEE Norchip Conference, pp. 1-4, November 2012.
- [33] J. Fritzin, C. Svensson, and A. Alvandpour, "A +32dBm 1.85GHz Class-D Outphasing RF PA in 130nm CMOS for WCDMA/LTE," in IEEE European Solid-State Circuits Conference (ESSCIRC), pp. 127-130, September 2011.
- [34] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.12-ENOB 1-kS/s SAR ADC in 0.13- μ m CMOS for Medical Implant Devices," in IEEE European Solid-State Circuits Conference (ESSCIRC), pp. 467-470, September 2011.
- [35] B. Mesgarzadeh, I. Esmail Zadeh, and A. Alvandpour, "A Multi-Segment Clocking Scheme to Reduce On-Chip EMI," in proc. IEEE International SoC Conference (SoCC), pp. 251-255, September 2011.
- [36] A. Fazli Yeknami, M. Savadi Osgooei, and A. Alvandpour, "A Programmable-Bandwidth Amplifier for Ultra-Low-Power Switched-Capacitor Application," in IEEE European Conference on Circuit Theory and Design (ECCTD), pp. 761-764, August 2011.
- [37] J. Fritzin, C. Svensson, and A. Alvandpour, "A Wideband Fully Integrated +30dBm Class-D Outphasing RF PA in 65nm CMOS," in IEEE International Symposium on Integrated Circuits (ISIC), December 2011.
- [38] E. Nilsson and C. Svensson, "Envelope detector sensitivity and blocking characteristics," in European Conference on Circuit Theory and Design (ECCTD), pp. 802-805, August 2011.
- [39] D. Zhang, C. Svensson, and A. Alvandpour, "Power Consumption Bounds for SAR ADCs," in IEEE European Conference on Circuit Theory and Design (ECCTD), pp. 556-559, August 2011.
- [40] A. Fazli Yeknami, M. Hansson, B. Mesgarzadeh, and A. Alvandpour, "A low voltage and process variation tolerant SRAM cell in 90-nm CMOS", in Proc. International Symp. on VLSI Design, Automation and Test (VLSI-DAT), pp. 78-81, 2010.
- [41] J. Fritzin, C. Svensson, and A. Alvandpour, "A Class-D Outphasing RF Amplifier with Harmonic Suppression in 90nm CMOS", in proc. IEEE European Solid-State Circuits Conference (ESSCIRC), pp. 310-313, September 2010.

- [42] J. Fritzin, T. Sundstrom, T. Johansson, and A. Alvandpour, "Reliability Study of a Low-Voltage Class-E Power Amplifier in 130nm CMOS", in proc. IEEE International Symposium on Circuits and Systems, (ISCAS), pp. 1907-1910, May 2010.
- [43] T. Sundstrom, C. Svensson, and A. Alvandpour, "A 2.4 GS/s, 4.9 ENOB at Nyquist, Single-Channel Pipeline ADC in 65nm CMOS, " in IEEE European Solid-State Circuits Conference (ESSCIRC), pp. 370-373, September 2010.
- [44] B. Mesgarzadeh and A. Alvandpour, "EMI reduction by resonant clock distribution networks", in proc. IEEE International Symposium on Circuits and Systems (ISCAS), pp. 977-980, May 2010.
- [45] O. E. Najari, T. Arnborg, and A. Alvandpour "Wideband Inductroless LNA Employing Simultaneous 2nd and 3rd Order Distortion Cancellation ", in proc. Norchip conference, Finland, 2010.
- [46] D. Zhang, A. Bhide, and A. Alvandpour, "Design of CMOS Sampling Switch for Ultra-Low Power ADCs for Biomedical Applications, " in proc. Norchip conference, Finland, 2010.
- [47] J. Fritzin and A. Alvandpour, "Low Voltage Class-E Power Amplifiers for DECT and Bluetooth in 130nm CMOS", in proc. IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), pp. 57-60, San Diego, USA, 2009.
- [48] B. Mesgarzadeh; M. Sadeghifar; P. Fredriksson; C. Jansson; F. Niklaus; A. Alvandpour, "A Low-noise Readout Circuit in 0.35- μ m CMOS for Low-cost Uncooled FPA Infrared Network Camera" SPIE conference, Defense, Security, and Sensing 2009: Infrared Technology and Applications XXXV, Vol. 7298, pp. 72982F1-72982F8, April 2009.
- [49] J. Fritzin, T. Johansson, and A. Alvandpour, "A 72.2Mbit/s LC-based Power Amplifier in 65nM CMOS for 2.4GHZ 802.11N WLAN", in proc. 15th Int. Conference Mixed Design of Integrated Circuit and Systems (MIXDES'08), pp. 155-158, Poznan, Poland, 2008.
- [50] B. Mesgarzadeh and A. Alvandpour, "A 2-GHz 7-mW Digital DLL-Based Frequency Multiplier in 90-nm CMOS", in proc. 34th European Solid-State Circuits Conference , Edinburgh, UK, pp. 86-89, 2008.
- [51] J. Fritzin, T. Johansson, and A. Alvandpour, "Impedance Matching Techniques in 65nm CMOS Power Amplifiers for 2.4GHz 802.11n WLAN", in proc. 38th IEEE European Microwave Conference (EuMC'08), pp. 1207-1210, Amsterdam, Netherlands, 2008.
- [52] J. Fritzin and A. Alvandpour, "A 72.2Mbit/s Transformer-Based Power Amplifier in 65nm CMOS for 2.4GHz 802.11n WLAN" in proc. IEEE NORCHIP Conference, pp. 53-56, Tallin, Estonia, 2008.
- [53] T. Sundström and A. Alvandpour "A 2.5-GS/s 30-mW 4-bit Flash ADC in 90nm CMOS", in proc. 26th Norchip conference, pp. 264-267, Tallin, Estonia, 2008.
- [54] S. Vangal, et al, "An 80-Tile 1.28TFLOPS Network-on-Chip in 65nm CMOS", in proceedings of IEEE International Solid State Circuits Conference (ISSCC'07), pp. 98-99, San Fransisco, USA, 2007.
- [55] S. Vangal, A. Singh, J. Howard, S. Dighe, N. Borkar, and A. Alvandpour, "A 5.1 GHz 0.34 mm² Router for Network-on-Chip Applications", 2007 Symposium on VLSI Circuits, Digest of Technical Papers, pp. 42-43, Kyoto, Japan, 2007.
- [56] M. Hansson, and A. Alvandpour, "Comparative analysis of process variation impact on flip flop power performance", in proc. IEEE International Symposium on Circuits and Systems, pp. 3744-3747, New Orleans, USA, 2007.

- [57] B. Mesgarzadeh, M. Hansson and A. Alvandpour, "Low-power bufferless resonant clock distribution networks", in proceedings of IEEE Meadwest Symposium on Circuits and Systems (MWSCAS'07), pp. 960-963, Montreal, Canada, 2007.
- [58] H. Fredriksson, C. Svensson, and A. Alvandpour, "A 3.4 GB/S low latency 1 bit input digital FIR-filter in 0.13 μ m CMOS", in proc. Mixed design of integrated circuits and systems (MIXDES'07), pp. 181-184, Ciechocinek, Poland, 2007.
- [59] T. Sundström, and A. Alvandpour, "A kick-back reduced comparator for a 4-6-bit 3-GS/S flash and in a 90nm CMOS process", in proc. Mixed design of integrated circuits and systems (MIXDES'07), pp. 195-198, Ciechocinek, Poland, 2007.
- [60] S. Andersson, I. Carlsson, S. Natarajan, and A. Alvandpour, "A 128Kb 5T SRAM in 0.18mm CMOS", International Conference on Memory Technology and Design (ICMTD'07), pp. 185-188, Giens, France, 2007.
- [61] M. Hansson, B. Mesgarzadeh, and A. Alvandpour, "1.56 GHz On-chip Resonant Clocking in 130nm CMOS", IEEE Custom Integrated Circuits Conference (CICC), September 2006, pp. 241-244.
- [62] B. Mesgarzadeh, M. Hansson, and A. Alvandpour, "Jitter Characteristic in Resonant Clock Distribution", European Solid-State Circuit Conference (ESSCIRC), Sept. 2006, pp. 464-467.
- [63] B. Mesgarzadeh and A. Alvandpour, "First-Harmonic Injection-Locked Ring Oscillators", IEEE Custom Integrated Circuits Conference (CICC), Sept. 2006, pp. 733-736.
- [64] M. Hansson and A. Alvandpour, "A Leakage Compensation Technique for Dynamic Latches and Flip-flops in Nano-scale CMOS", IEEE System-on-Chip Conference (SoCC), September 24-27 2006, pp. 83-84.
- [65] B. Mesgarzadeh and A. Alvandpour, "A 24-mW, 0.02-mm², 1.5-GHz DLL-Based Frequency Multiplier in 130-nm CMOS", IEEE Intl. System-on-Chip Conference (SoCC), Sept. 2006, pp. 257-260.
- [66] S. Hsu, M. Hansson, A. Agarwal, S. Mathew, A. Alvandpour, and R. Krishnamurthy, "A 9GHz 320x80bit Low Leakage Microcode Read Only Memory in 65nm CMOS", European Solid-State Circuit Conference (ESSCIRC), September 2006, pp 299-302.
- [67] B. Mesgarzadeh and A. Alvandpour, "A wide-tuning range 1.8 GHz quadrature VCO utilizing coupled ring oscillators", IEEE International Symposium on Circuits and Systems ISCAS, May 2006, pp. 5143-5146.
- [68] N. Mehmood, M. Hansson, and A. Alvandpour, "An Energy-Efficient 32-bit Multiplier Architecture in 90-nm CMOS", NORCHI conference, November 2006, pp 35-38.
- [69] K. Tom, A. Alvandpour, "Curvature compensated CMOS bandgap with sub 1V supply", IEEE International Workshop on Electronic Design, Test and Applications, Melbourne, Australia, 17-19 Jan. 2006.
- [70] M Hansson, A Alvandpour, S. Hsu, R. Krishnamurthy, "A process variation tolerant technique for sub-70nm latches and flip-flops", NORCHIP conference, Oulu, Finland, Nov 21-22, 2005, pp 149-152.
- [71] T. Sundström and A. Alvandpour, "A comparative analysis of logic styles for secure IC's against DPA attacks", NORCHIP conference, Oulu, Finland, Nov. 21-22, 2005, pp 297-300.
- [72] M Hansson and A Alvandpour, "Power-performance analysis of Sinusoidally clocked flip-flops", NORCHIP conference, Oulu, Finland, Nov 21-22, 2005, pp 153-156.

- [73] S. Vangal, N. Borkar, and A. Alvandpour, " A Six-Port 57GB/s Double-Pumped Nonblocking Router Core" 2005 International Symposium on VLSI Circuits, Kyoto, Japan, June 16-18, pp 268-269.
- [74] B. Mesgarzadeh, A. Alvandpour, "A Study of Injection Locking in Ring Oscillators", IEEE Symposium on Circuits and Systems, Kobe, Japan, May 23-26, 2005, pp 5465-5468.
- [75] H. Ohlsson, B. Mesgarzadeh, K. Johansson, O. Gustafsson, P. Löwenborg, H. Johansson, A. Alvandpour, "A 16 GSPS 0.18 μ m CMOS decimator for single-bit Sigma Delta -modulation", NORCHIP conference, pp. 175-178, Oslo, Norway, 8-9 November, 2004.
- [76] I. Carlson, S. Andersson, S. Natarajan, A. Alvandpour, "A high density, low leakage, 5T SRAM for embedded caches", European Solid-State Circuits Conference, ESSCIRC, pp. 215-222, Leuven, Belgium, September 21-23 2004.
- [77] P. Caputa, A. Alvandpour, C. Svensson, "High-speed on-chip interconnect modeling for circuit simulation", NORCHIP conference, pp. 143-146, Oslo, Norway, 8-9 November 2004.
- [78] M. Hansson, and A. Alvandpour, "A Low Clock Load Conditional Flip-flop", IEEE International System-on-Chip Conference, SoCC, pp. 169-170, Santa Clara, USA, 12-15 September 2004.
- [79] P. Caputa, H. Fredriksson, M. Hansson, S. Andersson, A. Alvandpour, and C. Svensson, "An Extended Transition Energy Cost Model for Buses in Deep Submicron Technologies", Forteenth International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2004, pp. 849-858, Santorini, Greece, September 15-17 2004.
- [80] B. Mesgarzadeh, C. Svensson, A. Alvandpour, "A New Mesochronous Clocking Scheme for Synchronization in SOC", IEEE Symp. on Circuits and Systems (ISCAS'04), pp. II -605-608, Vancouver, Canada, 23-26 May 2004.
- [81] A. Alvandpour, D. Somasekhar, R. Krishnamurthy, V. De, S. Borkar, C. Svensson, "Bitline Leakage Equalization for Sub-100nm Caches," European Solid State Circuits Conference, 2003, pp. 401-404.
- [82] M. Sinha, S. Hsu, A. Alvandpour, W. Burleson, R. Krishnamurthy, S. Borkar, " Low Voltage Sensing Techniques and Secondary Design Issues for sub-90nm Caches," European Solid State Circuits Conference, 2003, pp. 413-416.
- [83] M Hansson, Alvandpour A, "Crosstalk analysis considering power and delay on interconnects", Norchip 2003, Riga, Estland, Nov 10-11, pp 196-199, 2003.
- [84] A. Alvandpour, R. Krishnamurthy, D. Eckerbert, S. Apperson, B. Bloechel, S. Borkar, " A 3.5GHz 32mW 150nm Multiphase Clock Generator for High-Performance Microprocessors, " IEEE International Solid-State Circuits Conference, 2003, February 9, pp. 112-113.
- [85] C. H. Kim, K. Roy, S. Hsu, A. Alvandpour, R. Krishnamurthy, S. Borkar, "A Process Variation Compensating Technique for Sub-90nm Dynamic Circuits," International Symposium on VLSI Circuits, 2003, pp. 205-206.
- [86] S. Hsu, B. Chatterjee, M. Sachdev, A. Alvandpour, R. Krishnamurthy, S. Borkar, " A 90nm 6.5GHz 256x64b Dual Supply Register File with Split Decoder Scheme," International Symposium on VLSI Circuits, 2003, pp. 237-238.
- [87] M. Sinha, S. A. Alvandpour, W. Burleson, "High-Performance and Low-Voltage Sense-Amplifier Techniques for sub-90nm SRAM", IEEE International SOC conference, September 17-20, Portland, Oregon, 2003.

- [88] S.T. Oskulii, A Alvandpour, "Comparative study on low power, high performance standard cell flip flops", SPIE's International Symposium on Microelectronics, MEMS, pp 390-398, Perth, Australia, 9-12 December, 2003.
- [89] S. Natarajan, A. Alvandpour, "Ultra low power ferroelectric memory for SoC's", SPIE's international Symposium on Microelectronics, MEMS, pp 144-151, Perth, Australia, Dec, 2003.
- [90] A. Alvandpour, R. Krishnamurthy, S. Borkar, A. Rahman, C. Webb, " A burn-in tolerant dynamic circuit technique, " IEEE International Custom Integrated Circuits Conference, 2002, pp. 81 -84.
- [91] S. Hsu, A. Alvandpour, S. Mathew, S. Lu, R. Krishnamurthy, S. Borkar, "A 4.5GHz 130nm 32KB L0 Cache with a Self Reverse Bias Scheme," International Symposium on VLSI Circuits, 2002, pp. 48-49.
- [92] A. Alvandpour, R. Krishnamurthy, K. Sournyanath, S. Borkar, "A Low-Leakage Dynamic Multi-Ported Register file in 0.13mm CMOS, " International Symposium on Low Power Electronics and Design, pp. 2001, 68-71, 2001.
- [93] A. Alvandpour, R. Krishnamurthy, K. Soumyanath, S. Borkar, "A Conditional Keeper Technique for Sub-0.13mm Wide Dynamic Gates," International Symposium on VLSI Circuits, 2001, pp. 29-30.
- [94] R. Krishnamurthy, A. Alvandpour, G. Balamurugan, N. Shanbhag, K. Soumyanath, S. Borkar, "A 0.13um 6GHz 256x32b Leakage-tolerant Register File," International Symposium on VLSI Circuits, 2001, pp. 25-26.
- [95] P. Larsson-Edefors, H. Eriksson, D. Eckerbert, A. Alvandpour, "Low-Power Design of Delay-Constrained Circuits Using Dual-VT Process Technology" International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS, 2001, pp. 7.1.1-10.
- [96] A. Alvandpour, P. Larsson-Edefors, C. Svensson, " GLMC: Interconnect Length Estimation by Growth-Limited Multifold Clustering, " IEEE International Symposium on Circuits and Systems, Vol. 5, 2000, pp. 465- 46.
- [97] A. Alvandpour, P. Larsson-Edefors, C. Svensson, "A leakage-tolerant multi-phase keeper for wide domino circuits," IEEE International Conference on Electronics, Circuits, and System, Vol. 1, 1999, pp.209-212.
- [98] A. Alvandpour, P. Larsson-Edefors, C. Svensson, "Separation and Extraction of Short-Circuit Power Consumption in Digital CMOS VLSI circuits", International Symposium on Low Power Electronics and Design, 1998, pp. 245-249.
- [99] F. Mu, A. Alvandpour, C. Svensson, " Linearized Sub-optimum Method of Long Wire Interconnections with Uniform Wire Driver," IEEE International Symposium on Circuits and Systems, 1998, Vol. 2, pp. 252-255.
- [100] A. Alvandpour, P. Larsson-Edefors, C. Svensson, " Impact of Miller Capacitance on Power Consumption," International workshop on Power and Timing Modeling, Optimization and Simulation PATMOS, 1998, pp. 83-92.
- [101] A. Alvandpour, C. Svensson, "A Wire Capacitance Estimation Technique for Power Consuming Interconnections at High Levels of Abstraction," International workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS, 1997, pp. 305-314.
- [102] A. Alvandpour, C. Svensson, "Improving Cell libraries for Low Power Design," International workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS, 1996, pp. 317-325.

Invited papers and talks at international conferences

- [103] R. Krishnamurthy, A. Alvandpour, S. Mathew, M. Anders, S. Borkar, "High-performance, Low Power, and Leakage Tolerant Challenges for Sub-70nm Microprocessor Circuits," European Solid-State Circuit Conference, 2002.
- [104] R. Krishnamurthy, A. Alvandpour, V. De, S. Borkar, "High-performance and Low-power Challenges for Sub-70nm Microprocessor Circuits," IEEE Custom Integrated Circuits Conference, 2002, pp. 125-128.
- [105] C. Svensson, A. Alvandpour, "Low power and Low voltage CMOS Digital Circuit Techniques," International symposium on Low Power Electronics and Design, 1998 pp. 7-10.
- [106] S. Natarajan and A. Alvandpour, "Emerging memory technologies– mainstream or hearsay?", IEEE VLSI-TSA International Symposium on VLSI Design, Hsinchu, Taiwan, April 25-29, 2005, pp 222-228.
- [107] S. Natarajan, A. Alvandpour, "Mainstream Memory Technologies in Deep Submicron", 12th IEEE Mediterranean Electrotechnical Conference, MELECON, pp. 175-178, Dubrovnik, Croatia, 12-15 May 2004.
- [108] S. Natarajan, A. Alvandpour, " High performance and SER insensitive memories", SPIE's International Symposium on Microelectronics, MWMS, and Nanotechnology, Perth, Australia, 9-12 December, 2003.
- [109] S. Natarajan, A. Alvandpour, "SoC versus SIP: What makes sense?", " SPIE's International Symposium on Microelectronics, MWMS, and Nanotechnology, Perth, Australia, 9-12 December 2003.
- [110] A. Alvandpour, "High-Performance and Low-Power Challenges for Sub-70nm Systems on Chip" International workshop on Circuit Design (IWCD'2004), June 17, 2004, National Taiwan University, Taipei, Taiwan.
- [111] A. Alvandpour, S. Mathew, "Advanced high-performance microprocessor design challenges and solutions," ASIC/SOC Conference, 2002. 15th Annual IEEE International, 2002, pp. 476 - 476.
- [112] A. Alvandpour, "High-performance and Low-voltage Datapath and Interconnect Design Challenges", 12th IEEE Mediterranean Electrotechnical Conference, MELECON, 2004, May 12-15, Dubrovnik Croatia.

Patents

- [1] U.S. Patent No: 7,053,663, " Dynamic gate with conditional keeper for soft error rate reduction "
Issued: May 30, 2006
Inventors: P. Hazucha, A. Alvandpour, R. Krishnamurthy, T. Karnik
- [2] U.S. Patent No: 7,002,389, " Fast static receiver with input dependent inversion threshold "
Issued: Februrary 21, 2006.
Inventors: A. Alvandpour, R. Krishnamurthy
- [3] U.S. Patent No: 6,919,737, " Voltage-level converter "
Issued: July, 2005
Inventors: A. Alvandpour, R. Krishnamurthy

- [4] U.S. Patent No: 6,838,910, " Fast dual-rail dynamic logic style "Issued: January 4, 2005Inventors: A. Alvandpour, P. Larsson-Edefors, R. Krishnamurthy, K. Soumyanath
- [5] U.S. Patent, No: 6,847,569, " Differential current sense amplifier "Issued: January 25, 2005Inventors: S. Manoj, R. Krishnamurthy, A. Alvandpour
- [6] U.S. Patent No: 6,791,364, " Conditional burn-in keeper for dynamic circuits "Issued: September 14, 2004Inventors: A. Alvandpour, R. Krishnamurthy
- [7] U.S. Patent No: 6,751,141, " Differential charge transfer sense amplifier "Issued: June 15, 2004Inventors: A. Alvandpour, S. Manoj, R. Krishnamurthy
- [8] U.S. Patent No: 6,707,708, "Static random access memory with symmetric leakage-compensated bit line"Issued: March 16, 2004Inventors: A. Alvandpour, D. Somasekhar, S. Hsu, R. Krishnamurthy, V. De
- [9] U.S. Patent No: 6,690,205, "Enhanced domino circuit"Issued: February 10, 2004Inventors: A. Alvandpour
- [10] U.S. Patent No: 6,717,441, " Flash [II]-Domino: a fast dual-rail dynamic logic style"Issued: April 6, 2004Inventors: A. Alvandpour, P. Larsson-Edefors, R. Krishnamurthy, K. Soumyanath
- [11] U.S. Patent No: 6,633,190, "Multi-phase clock generation and synchronization"Issued: October 14, 2003Inventors: A. Alvandpour, D. Eckerbert; Daniel, R. Krishnamurthy
- [12] U.S. Patent No: 6,617,890, "Measuring power supply stability"Issued: September 9, 2003Inventors: T. Chen, P. Hazucha, A. Alvandpour; T. Karnik, C. Chen
- [13] U.S. Patent No: 6,614,680, "Current leakage reduction for loaded bit-lines in on-chip memory structures"Issued: September 2, 2003Inventors: A. Alvandpour, R. Krishnamurthy, S. Narendra
- [14] U.S. Patent No: 6,590,801, "Current leakage reduction for loaded bit-lines in on-chip memory structures"Issued: July 8, 2003Inventors: A. Alvandpour, R. Krishnamurthy, S. Narendra
- [15] U.S. Patent No: 6,559,492, "On-die switching power converter with stepped switch drivers and method"Issued: May 6, 2003Inventors: P- Hazucha, A. Alvandpour
- [16] U.S. Patent No: 6,549,040, "Leakage-tolerant keeper with dual output generation capability for deep sub-micron wide domino gates "Issued: April 15, 2003Inventors: A. Alvandpour, K. Soumyanath, R. Krishnamurthy,
- [17] U.S. Patent No: 6,519,178, "Current leakage reduction for loaded bit-lines in on-chip memory structures"

- Issued: February 11, 2003
Inventors: A. Alvandpour, R. Krishnamurthy, S. Narendra
- [18] U.S. Patent No: 6,510,077, "Current leakage reduction for loaded bit-lines in on-chip memory structures"
Issued: January 21, 2003
Inventors: A. Alvandpour, R. Krishnamurthy, S. Narendra
- [19] U.S. Patent No: 6,351,150, "Low switching activity dynamic driver for high performance interconnects"
Issued: February 26, 2002
Inventor: R. Krishnamurthy; M. Anders, A. Alvandpour
- [20] U.S. Patent No: 6,498,514, "Domino circuit"
Issued: December 24, 2002
Inventors: A. Alvandpour
- [21] U.S. Patent No: 6,493,254, "Current leakage reduction for loaded bit-lines in on-chip memory structures"
Issued: December 10, 2002
Inventors: A. Alvandpour, R. Krishnamurthy, S. Narendra
- [22] U.S. Patent No: 6,388,940, "Leakage-tolerant circuit and method for large register files "
Issued: May 14, 2002
Inventors: A. Alvandpour; G. Balamurugan, K. Soumyanath, R. Krishnamurthy
- [23] U.S. Patent No: 6,353,342, "Integrated circuit bus architecture including a full-swing, clocked, common-gate receiver for fast on-chip signal transmission"
Issued: March 5, 2002
Inventors: A. Alvandpour; K. Soumyanath, R. Krishnamurthy
- [24] U.S. Patent No: 6,137,319, "Reference-free single ended clocked sense amplifier circuit"
Issued: October 24, 2000
Inventors: R. Krishnamurthy; A. Alvandpour, R. Spotten.