Analog power modeling

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Outline

Analog power consumption
Sampling power
The transistor
Accuracy
AD converter power consumption
Relevance for radio
Conclusion

STRINGENT

Analog power consumption

Digital power consumption is very well understood today:

Switching power = $f_c V_{dd}^2 \Sigma \alpha_i C_i$, C_i technology dependent

Analog power consumption much less understood

Depends on dynamic range (DR), noise level, accuracy. ~$kTf_s DR$

To a less extent technology dependent (if far from performance limits)

We will investigate analog power consumption with AD-converters as an example

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Analog power consumption

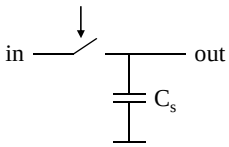
Why power modeling?

Understanding power consumption facilitates high level power savings, through architecture selection, topology selection, bias selection…

A lower bound to power consumption facilitates selection of research areas or selection of which blocks to optimize

Sampling power

A lower power limit - consider only the sampling



Noise voltage generated: $v_{nS}^2 = \frac{kT}{C_s}$

Maximum sine voltage with supply voltage V_{FS}:

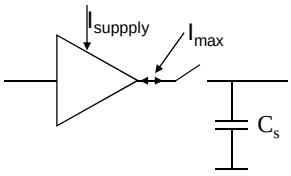
$v_s^2 = \frac{V_{FS}^2}{8}$ gives dynamic range: $DR = \frac{v_s^2}{v_{nS}^2} = \frac{V_{FS}^2 C_s}{8kT}$

or, capacitance needed: $C_S = \frac{8kTDR}{V_{FS}^2}$

To drive the capacitor we need a current of $I=C_sV_{FS}f_s$,

leading to a power consumption of $P_S = IV_{FS} = 8kTf_sDR$

Sampling power



Assumption: $I_{supply} = I_{max}$

Using the dynamic range of a quantization noise limited AD-converter, $DR=3/2\ 2^{2n}$, we can also write:

$P_S = 12kTf_s 2^{2n}$

Sampling power

$$P_S = IV_{FS} = 8kTf_sDR$$

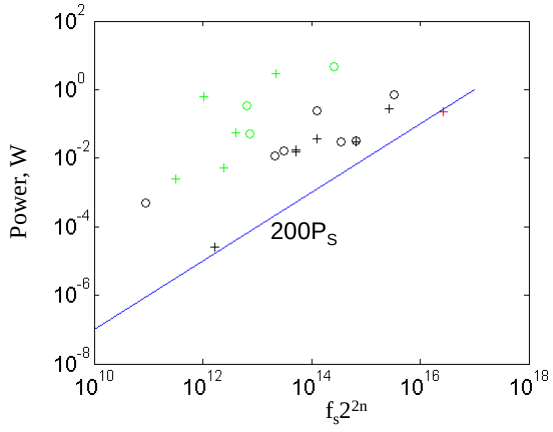
This expression is valid for any switched capacitor circuit
(Example a first order switched capacitor filter)
First described by Vittoz 1990.

Note that this expression is *independent of technology*

Note that this expression is *independent of supply voltage*

Note that this expression is proportional to 2^{2n},
whereas a digital system power is proportional to n.
We expect digital to have lower power at high n or DR.

Sampling power



Examples of experimental AD converter power consumptions

(Svensson, Andersson Bogner, NORCHIP 2006)

Sampling power

Check capacitor values (V_{FS}=1V)

$$C_s = \frac{12kT}{V_{FS}^2} 2^{2n}$$

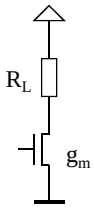
n	C_s
4	13aF
6	0.2fF
8	3fF
10	52fF
12	0.8pF
14	13pF
16	214pF

Minimum transistor gate capacitance about 0.9fF in 0.18µm process)

Below 8b dynamic range we can not reach noise limiting capacitance
⇒ Power limited by technology (C_{min})

13pF quite high (6000µm² MIM area)

The transistor



Drain noise current: $i_{nD}^2 = 4kT\gamma g_m B$

Equivalent input noise: $v_{nG}^2 = 4kT\gamma \frac{1}{g_m} B$

Dynamic range: $DR = \frac{V_{FS}^2}{8} \frac{g_m}{4kT\gamma B}$

Required g_m for dynamic range DR: $g_m = \frac{32kT\gamma B}{V_{FS}^2} DR$

Required drain current: $I_D = g_m V_{eff}$

Power consumption: $P = IV_{FS} = 32kT\gamma B \frac{V_{eff}}{V_{FS}} DR$ ($P_S = 8kTf_s DR$)

The transistor

A note on V_{eff}

Definition: $V_{eff}=I_D/g_m$

Bipolar transistor: $V_{eff}=kT/q$ (and $\gamma=1/2$)

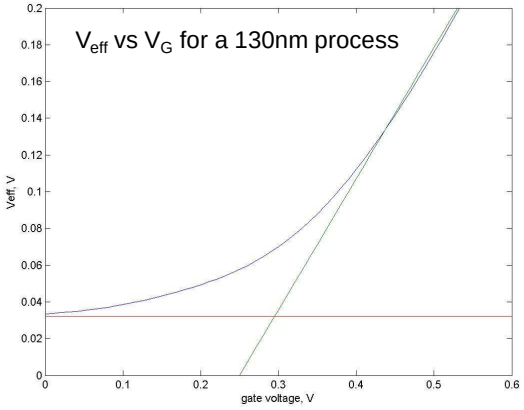
Long channel MOST: $V_{eff}=(V_G-V_T)/2$ (and $\gamma=2/3$)

Long channel MOST in subthreshold: $V_{eff}=mkT/q$, m=1.2…1.5

Submicron MOST: $V_{eff} \approx mkT/q + k_1 I_D$ (transition region)

The transistor

A note on V_{eff}



The transistor

A note on supply voltage

(We have assumed supply voltage = V_{FS})

Power proportional to V_{eff}/V_{FS}

Classical CMOS, this relation was kept constant
(V_{FS} (V_{dd}), V_G and V_T scaled with process scaling)

Submicron CMOS, V_{eff} is reduced very slowly.
Power increases with reduced supply voltage! (Annema et. al.)

The transistor

A note on LNA's

Noise figure, NF, given by $NF = 1 + \frac{v_{ng}^2}{kTR_0B} = 1 + \frac{4\gamma}{g_m R_0}$

R_0 is the input impedance level (normally 50Ω)
Required g_m for noise figure NF leads to power consumption:

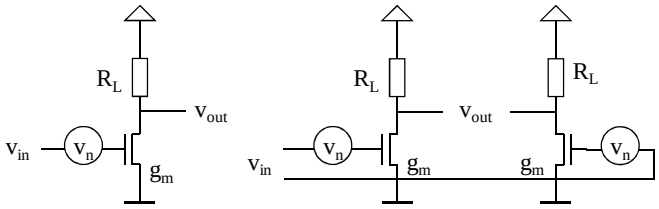
$$P = \frac{4\gamma V_{FS} V_{eff}}{R_0 (NF - 1)}$$

γ=1.5, V_{FS}=1V, V_{eff}=80mV, R_0=50Ω, NF=3dB
P=9.6mW

For narrow-band circuits we may transform the external impedance to a larger impedance at transistor input (larger R_0, smaller power)
Power increases with increased supply voltage!

The transistor

A note on differential circuits



Same transistors, same bias, same signal per transistor

$$DR_{diff} = \frac{(2v_{in})^2}{2v_n^2} = 2DR_{SE} \qquad P_{diff} = 2P_{SE}$$

Same dynamic range
Same power

The transistor

A note on g_m constraints

We have shown that P~V_{eff}, so why not choosing minimum V_{eff} (mkT/q) ?

For a given transistor size, we have a fixed C_G and g_m=f(I_D).

Transistor speed capability can be described by $f_T=g_m/2\pi C_G$

If we need to utilize transistor speed capability, we need larger g_m.
Note that g_m has a maximum in submicron devices, *keep I_D low*!

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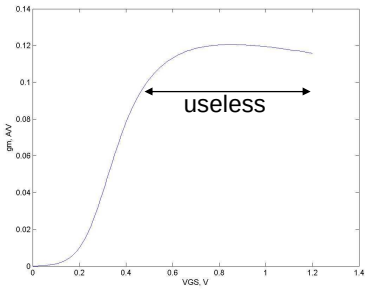
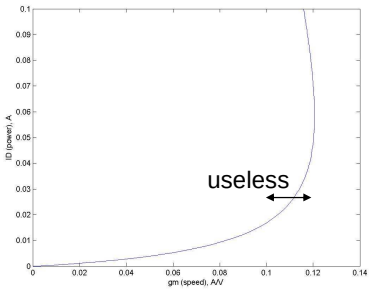
The transistor

A note on g_m constraints



g_m vs V_{GS} (130nm process)



I_D vs g_m (speed) (130nm process)

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Accuracy

Asume that gain is controlled by a capacitance ratio

Gain $G = \frac{C_2}{C_1}$ gives gain variance: $\left(\frac{\sigma_G}{G}\right)^2 = \left(\frac{\sigma_{C1}}{C_1}\right)^2 + \left(\frac{\sigma_{C2}}{C_2}\right)^2$

Relative capacitance variance: $\frac{\sigma_C}{C} = \frac{C_{mm}}{\sqrt{2C}}$ (C_{mm} is a process parameter)

Gain variance: $\left(\frac{\sigma_G}{G}\right)^2 = \frac{C_{mm}^2}{2C_p}$ where $C_p = \frac{C_1 C_2}{C_1 + C_2}$

Make relative gain error (assumed twice the variance) equal to 1LSB:

$$\frac{\Delta G}{G} = \frac{2\sigma_G}{G} = \frac{2C_{mm}}{\sqrt{2C_p}} = 2^{-n}$$

Required C_p: $C_p = 2C_{mm}^2 2^{2n}$

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Accuracy

Comparison to noise limited capacitance

$C_{mm}=4\cdot10^{-10}$ $F^{1/2}$ (130nm process)

$$C_s = \frac{12kT}{V_{FS}^2}2^{2n} \qquad C_p = 2C_{mm}^2 2^{2n}$$

n	C	C
8	3fF	18fF
10	52fF	290fF
12	0.8pF	4.6pF
14	13pF	73pF

Unclear how C_{mm} scales (this value is for MIM capacitor)

Capacitor 6.4 times larger because of matching, gives 6.4 times larger power

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AD converter power

General

We will look at pipelined and flash converters

We will assume redundancy and error correction; no need for accuracy

We start with noise limited converters, then add process limitations

We compare with published Data

AD converter power

The comparator (noise limited)

A comparator is in principle a high gain stage, limited by the noise level in the beginning of the comparison process. Let us assume a drain noise current in the first stage of i_{dg}, and a drain circuit noise bandwidth of $1/(4R_LC_L)$:

$$i_{dn}^2 = 4kT\gamma g_m \frac{1}{4R_L C_L}$$

Let us define the open loop gain of the amplifier, $\beta=g_mR_L$. Then we have the equivalent input noise voltage from $v_{nC}=i_{dn}/g_m$:

$$v_{nC}^2 = \frac{\gamma kT}{\beta C_L}$$

Equalizing this noise to a fraction, α, of the quantization noise gives minimum capacitance:

$$C_{Ln} = \frac{12\gamma kT}{\alpha\beta V_{FS}^2} 2^{2n} \qquad \left(\text{quantization noise: } v_{qn}^2 = \frac{V_{FS}^2}{12} 2^{-2n} \right)$$

AD converter power

The comparator (noise limited)

Speed is controlled by $\tau=C_L/g_m$ and that the comparator must resolve $V_{FS}2^{-n}$ Within decision time, T_d:

$$V_{FS} 2^{-n} e^{\frac{T_d}{\tau}} = V_{FS}$$

With decision time $T_d=1/2f_s$ the minimum gm is given by:

$$g_m = 2nf_s C_{Ln} \ln 2$$

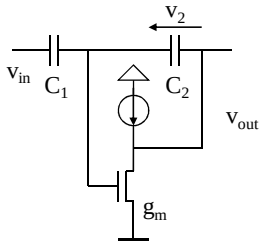
This required g_m gives the supply current of g_mV_{eff} and a power consumption:

$$P_C = 4nf_s C_{Ln} V_{FS} V_{eff} \ln 2$$

With $\gamma=2$, $\beta=10$, $V_{eff}=80$mV, $V_{FS}=1.5$V, n=14, $\alpha=0.5$, $P_C \approx P_S$

AD converter power

A switched capacitor amplifier (noise limited)



In evaluation

Noise contribution
α*(quantization noise)

After evaluation, C_2 is isolated and V_2 is the output voltage

$$v_2 = \frac{C_1}{C_2}\frac{v_{in}}{1+ j\omega\frac{C_1}{g_m}}$$

Equivalent input noise voltage:

$$v_{gn}^2 = \frac{i_{dn}^2}{g_m^2} = \frac{4kT\gamma g_m}{g_m^2}\frac{g_m}{4C_1} = \frac{kT\gamma}{C_1}$$

Required capacitance

$$C_1 = \frac{12\gamma kT}{\alpha V_{FS}^2}2^{2n}$$

AD converter power

A switched capacitor amplifier (noise limited)

Settling to 2^{-n} within time T_{se}; timeconstant $\tau=C_1/g_m$: $e^{-\frac{T_s}{\tau}} = 2^{-n}$

Gives g_m need and supply current $I_{Ase}=g_mV_{eff}$: $I_{Ase} = \frac{C_1V_{eff}n\ln(2)}{T_{se}}$

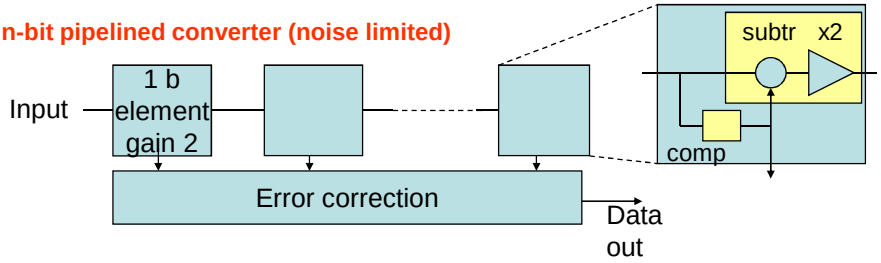
Slewing to V_{FS} within time T_{sl} need current: $I_{Asl} = \frac{C_2V_{FS}}{T_{sl}}$

Making currents equal under constraint $T_{se}+T_{sl}=1/2f_s$ gives:

$$P_A = f_sC_1V_{FS}^2\left(1+2n\frac{V_{eff}}{V_{FS}}\ln 2\right)$$

AD converter power

n-bit pipelined converter (noise limited)



We assume 1bit per stage redundant converter.
n-bit pipelined converter uses *n comparators* and *n operational amplifiers*.
Resolution is reduced by 1bit per stage and comparator can be minimum.
(noise removed through redundancy)

$$P_{pipe} = nP_{C\min} + P_A \sum_0^{n-1} 2^{-i} \approx 2P_A$$

AD converter power

n-bit pipelined converter (complete)

Comparator power (min capacitance):
(C_{min} is minimum transistor gate capacitance)

$$P_C = 4nf_s C_{\min} V_{FS} V_{eff} \ln 2$$

Amplifier power
(i is stage no from input)

$$P_A = f_s V_{FS}^2 \left(1 + 2n \frac{V_{eff}}{V_{FS}} \ln 2\right) \max(C_{\min}, C_1 2^{-i})$$

$$P_{pipe} = nP_{C\min} + \sum_0^{n-2} P_A \approx nP_{C\min} + f_s V_{FS}^2 \left(1 + 2n \ln 2 \frac{V_{eff}}{V_{FS}}\right)(nC_{\min} + 2C_1)$$

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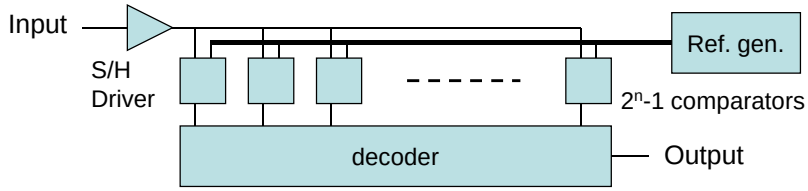
AD converter power

n-bit flash converter (noise limited)



n-bit flash converter uses 1 sampling circuit (or driver) and 2^n-1 comparators.

$$P_{flash} = f_s C_s V_{FS}^2 + (2^n - 1) P_C$$ with $C_s=(2^n-1)C_{Ln}$

(Reasonable to assume C_s dominant over noise limited capacitance)

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AD converter power

n-bit flash converter (complete)

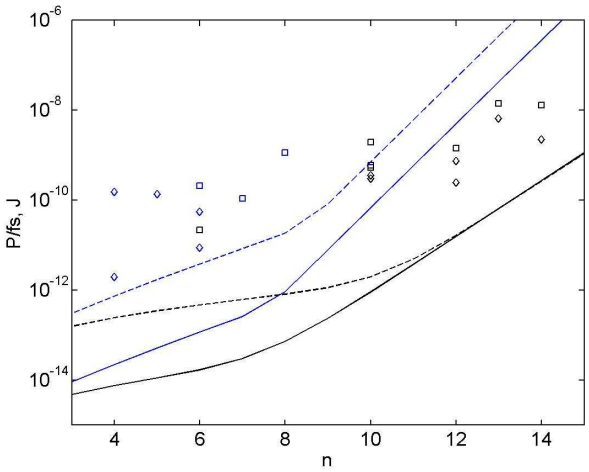
n-bit flash converter uses 1 sampling circuit (or driver) and 2^n-1 comparators.

$$P_{flash} = f_s C_s V_{FS}^2 + (2^n - 1) P_C$$

with $C_s=(2^n-1)\max(C_{min},C_{Ln})$ and $P_C = 4nf_s \max(C_{\min}, C_{Ln}) V_{FS} V_{eff} \ln 2$

$$P_{flash} = f_s \left(V_{FS}^2 C_{\min} + \frac{24\gamma kT}{\beta} 2^{2n} \right) (2^n - 1) \left(1 + 4n \ln 2 \frac{V_{eff}}{V_{FS}} \right)$$

AD converter power



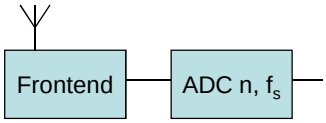
Experimental data
Nominal n

black pipe
blue flash
full 90nm
dashed 0.35µm

Isscc:
square 2002
diamond 2006

90nm	*0.35µm*
0.8fF	*2.5nF*
1.0V	*3.3V*
80mV	*250mV*

Relevance for radio



Blocker (1W, 1m) $P_B = \frac{A_{antenna}}{4\pi R^2} P_{transmitblocker} \approx 0.1mW$

Thermal noise spectral density $S_t = FkT$

Together determines ADC requirements $f_s 2^{2n} = \frac{4}{3}\frac{P_B}{FkT}$

F=2 (3dB) we get $f_s 2^{2n} = 1.6 \cdot 10^{16}$ Hz

(P_S=0.8mW; 100P_S=80mW)

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Conclusion

Power consumption of an analog sampler gives good insight in analog power consumption ($P \sim kTf_s 2^{2n}$; $P \sim kTf_{BW}DR$)

Basic analog power consumption independent of technology

Technology limitations show up at low dynamic range

Power saving by replacing analog precision by digital error correction

Power savings by proper choice of operating point

$f_s 2^{2n}$ is also a relevant performance measure for radio

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