On Analog Power Consumption

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Elliit 2010

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Outline

Introduction

Basics of analog power consumption

Comparison to digital

Further work

Application: ADC

Conclusions

Introduction

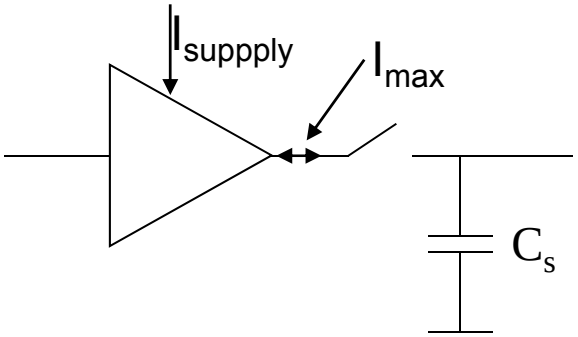
Analog power consumption is complex and badly understood

Text books and practice specialize on performance constraints rather than power

This is an attempt to address analog design for low power and to define lower bounds to analog power consumption

Basics of analog power consumption

Ideal sampler



Noise voltage generated: $v_{nS}^2 = \frac{kT}{C_s}$

Maximum sine voltage with supply voltage V_{FS}:

$v_s^2 = \frac{V_{FS}^2}{8}$ Gives dynamic range: $DR = \frac{v_s^2}{v_{nS}^2} = \frac{V_{FS}^2 C_s}{8kT}$

or, capacitance needed: $C_S = \frac{8kTDR}{V_{FS}^2}$

To drive the capacitor we need a current of $I=C_s V_{FS} 2f_s$,

leading to a power consumption of $P_S = IV_{FS} = 16kTf_s DR$

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Basics of analog power consumption

Ideal sampler

$$P_S = IV_{FS} = 16kTf_sDR$$

This expression is valid for any switched capacitor circuit
(Example a first order switched capacitor filter)
First described by Vittoz 1990.

Note that this expression is *independent of technology*

Note that this expression is *independent of supply voltage*
(but assumed V_{FS}=V_{dd}; V_{dd} is supply voltage)

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Basics of analog power consumption

Ideal sampler - impact of technology

In the above derivation we used $C_S = \frac{8kTDR}{V_{FS}^2}$

But C_s can not be made smaller than the smallest capacitance of the actual technology, C_{min}.

So actually we should use $C=\max(C_s, C_{min})$ in power estimation.

In the following we use the input capacitance of a minimum inverter as C_{min}. $C_{min}=4*C_{gn}$. C_{gn} will scale with technology as the feature size (half feature size - half capacitance)

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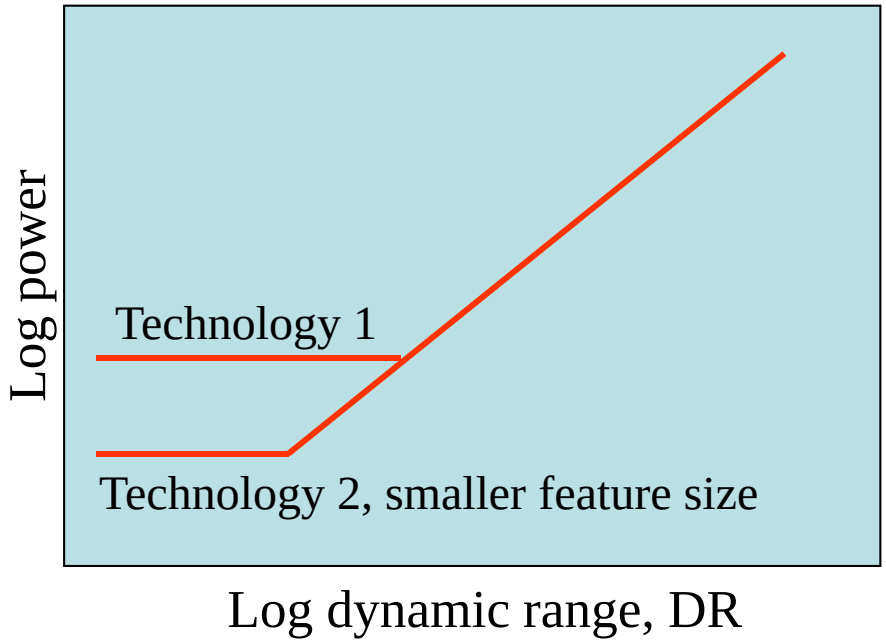
Basics of analog power consumption

Ideal sampler - impact of technology

Large DR - independent technology

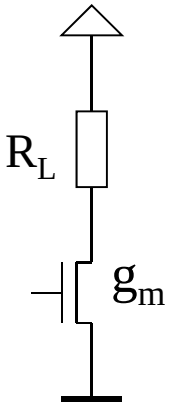
Smaller DR - technology dependent
Smaller feature size - less power

Note, scaled as (feature size)^3
($P_S \sim V_{FS}^2 C_{min}$)



Basics of analog power consumption

The transistor



Drain noise current: $i_{nD}^2 = 4kT\gamma g_m B$

Equivalent input noise: $v_{nG}^2 = 4kT\gamma \frac{1}{g_m} B$

Dynamic range: $DR = \frac{V_{FS}^2}{8} \frac{g_m}{4kT\gamma B}$

Required g_m for dynamic range DR: $g_m = \frac{32kT\gamma B}{V_{FS}^2} DR$

Required drain current: $I_D = g_m V_{eff}$

Power consumption: $P = IV_{FS} = 32kT\gamma B \frac{V_{eff}}{V_{FS}} DR$ (compare $P_S = 16kTf_s DR$)

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Basics of analog power consumption

The transistor – a note on V_{eff} and γ

V_{eff} definition: $V_{eff}=I_D/g_m$ γ defined from noise measurements

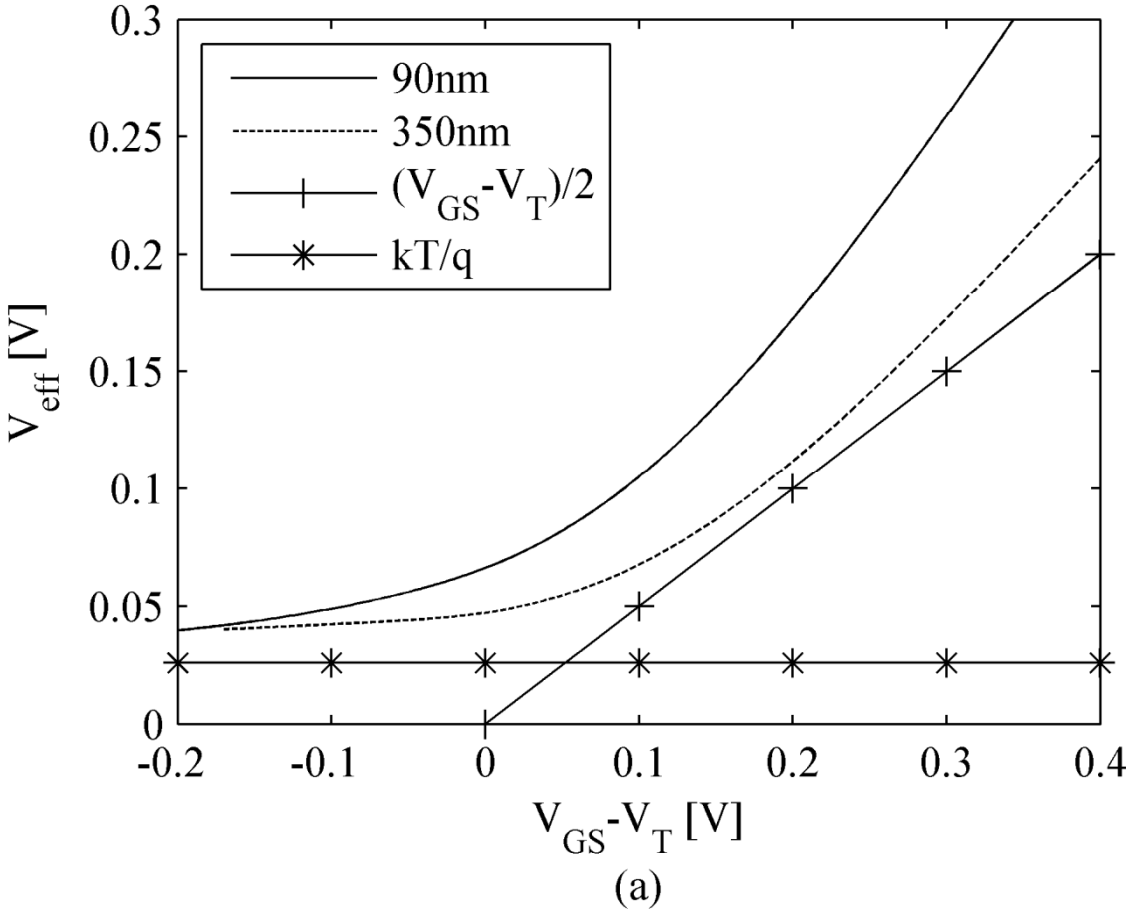
Bipolar transistor: $V_{eff}=kT/q$ $\gamma=1/2$ (shot noise)

Long channel MOST: $V_{eff}=(V_G-V_T)/2$ $\gamma=2/3$ (resistance noise)

Long channel MOST in subthreshold: $V_{eff}=mkT/q$, m=1.2…1.5

Submicron MOST: V_{eff} in transition region γ~1.5-2

Basics of analog power consumption



V_{eff} vs V_G for
a 90nm process
a 350 nm process

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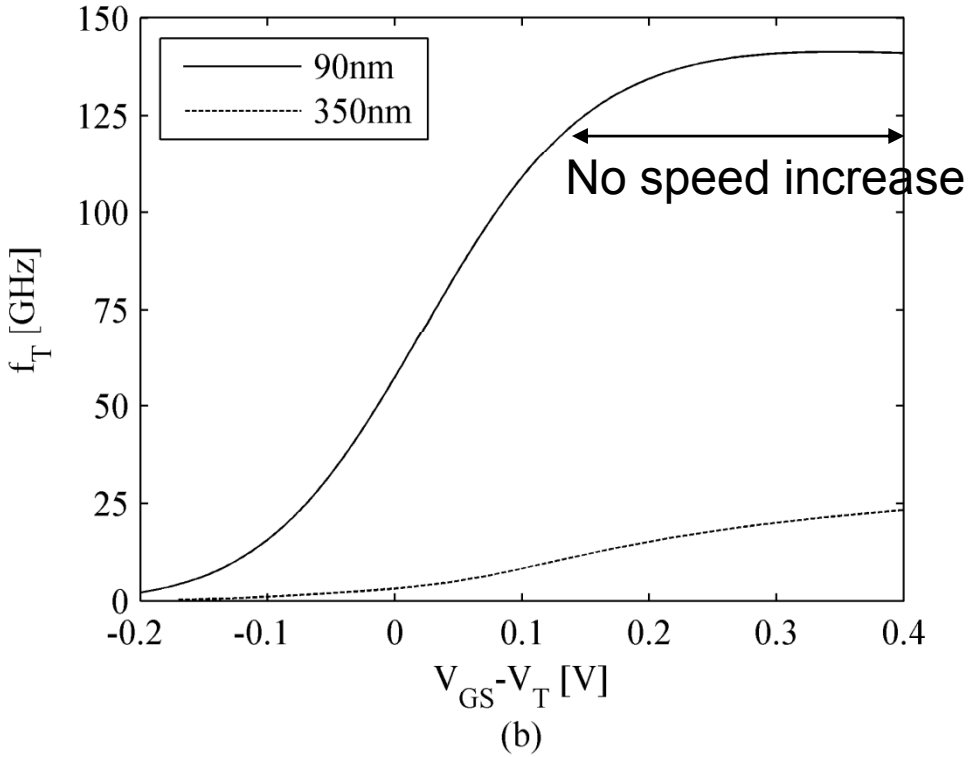
The transistor – a note on V_{eff} and speed.

Speed controlled by f_T

$f_T=g_m/2\pi C_g$



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The transistor – a note on V_{eff} and input swing

For a linear transistor behaviour we expect a limited drain current variation, say $I_{DC} \pm \Delta I_d = I_{DC} \pm I_{DC}/2$, with $I_{DC}=g_m V_{eff}$.

We then have $\Delta V_g=\Delta i_d/g_m=V_{eff}/2$, or $V_{FSin}=2\Delta V_g=V_{eff}$

High linearity may require lower swing, $V_{FSin} < V_{eff}$

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The transistor – a note on V_{dd}

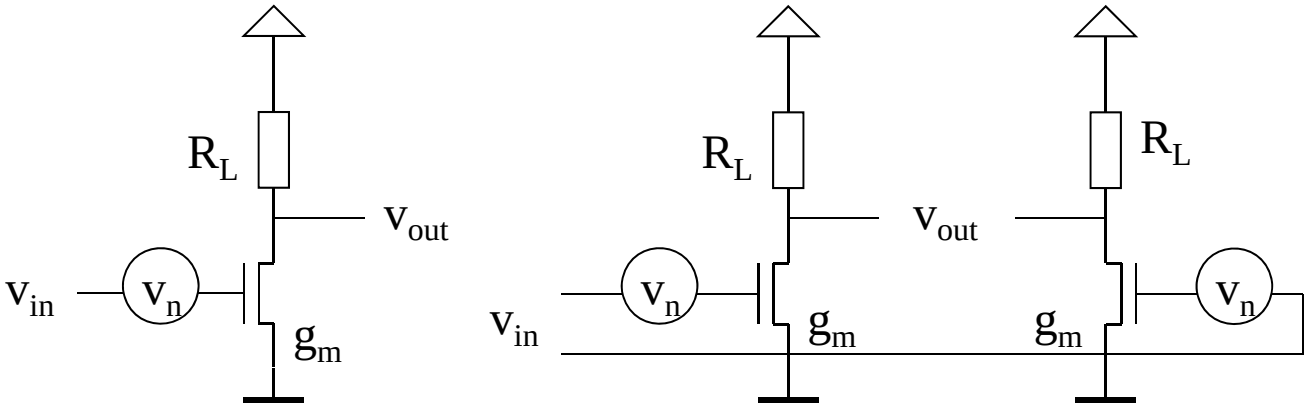
We assumed supply voltage = V_{FS}

With higher supply, V_{dd}, we define voltage efficiency $\eta_v = V_{FS}/V_{dd}$

Then power *increases* by $1/\eta_v$

Basics of analog power consumption

The transistor – a note on differential circuits



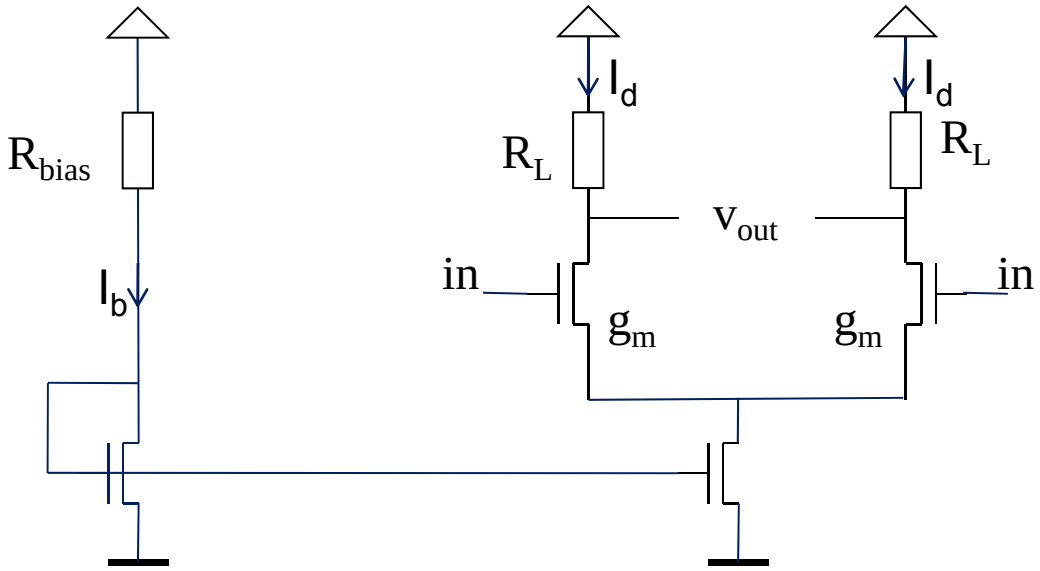
Same transistors, same bias, same signal per transistor

$$DR_{diff} = \frac{(2v_{in})^2}{2v_n^2} = 2DR_{SE} \qquad P_{diff} = 2P_{SE}$$

Same dynamic range
Same power

Basics of analog power consumption

The transistor – a note on bias circuits



Current efficiency, $\eta_I = 2I_d/(I_b+2I_d)$. Note, I_b may need to be large for eg. low noise

Note – bias circuit may be shared

Basics of analog power consumption

The transistor – impact of technology

Regarding minimum g_m.
We can always reduce g_m to adapt to DR by reducing V_G.
BUT this leads to small V_{eff}, which may limit speed or input swing
Maybe we will have g_{mmin} and I_{DCmin}.

Power proportional to V_{eff}/V_{FS}

Classical CMOS, this relation was kept constant
V_{FS} (V_{dd}), V_G and V_T scaled with process scaling

Submicron CMOS, V_{eff} is reduced very slowly.
So power may *increase* with reduced supply voltage! (Annema et. al.)

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Basics of analog power consumption

The transistor – a conclusion

A transistor amplifier (single ended or differential) uses power:

$$P = IV_{FS} = 32kT\gamma B\frac{V_{eff}}{V_{FS}}DR$$

This is constrained by:

Increased by $1/\eta_v$ for $V_{FS}<V_{dd}$
Increased by $1/\eta_i$ for extra currents (eg. bias)
V_{eff} must be large enough for transistor speed ($f_T=g_m/2\pi C_g$ large enough)
V_{eff} must exceed input swing, V_{FSin}, related to linearity requirements
Technology dependence at low DR - complex

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Comparison to digital

Comparison to analog

Consider a single pole filter / 1-tap FIR filter

Analog, use transistor formula:
(with DR=3●2^{2n}/2; B=f_s/2)

$$P_a = 24kT\gamma \frac{V_{eff}}{V_{FS}} f_s 2^{2n}$$

Digital. Need 1 m-coefficient, n-bit multiplier plus 1 n-bit adder
Multiplier uses m adders; 1 adder use n FAs (full adders); each FA uses equivalent 9 inverters, ie. C=9C_{min}. Totally 9(m+1)nC_{min},
With m=6 we have 63nC_{min}.

$$P_d = \frac{1}{2}\alpha f_c 63nC_{\min}V_{dd}^2$$

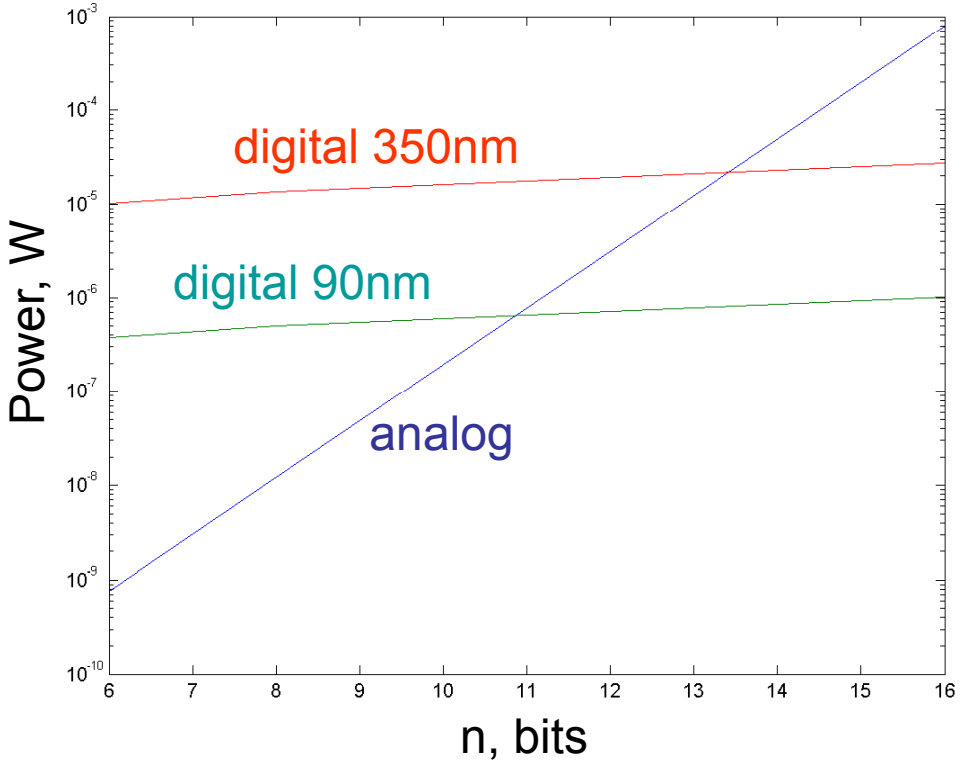
Comparison to digital

Comparison to analog

f_s=20MHz
γ=1.5
$V_{eff}=0.1V_{FS}$

90nm: V_{dd}=1V
C_{min}=1fF
α=0.1

350nm V_{dd}=3V
C_{min}=3fF
α=0.1



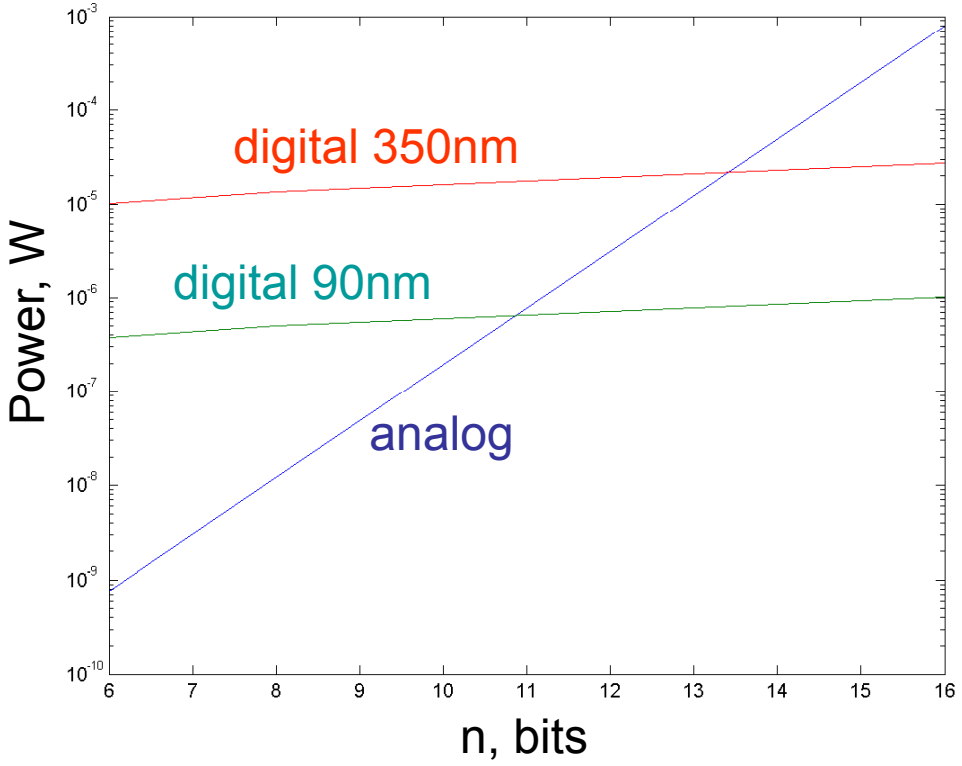
Comparison to digital

Comparison to analog

Analog preferred for low DR

Digital preferred for large DR

Digital improved by scaling



Further work

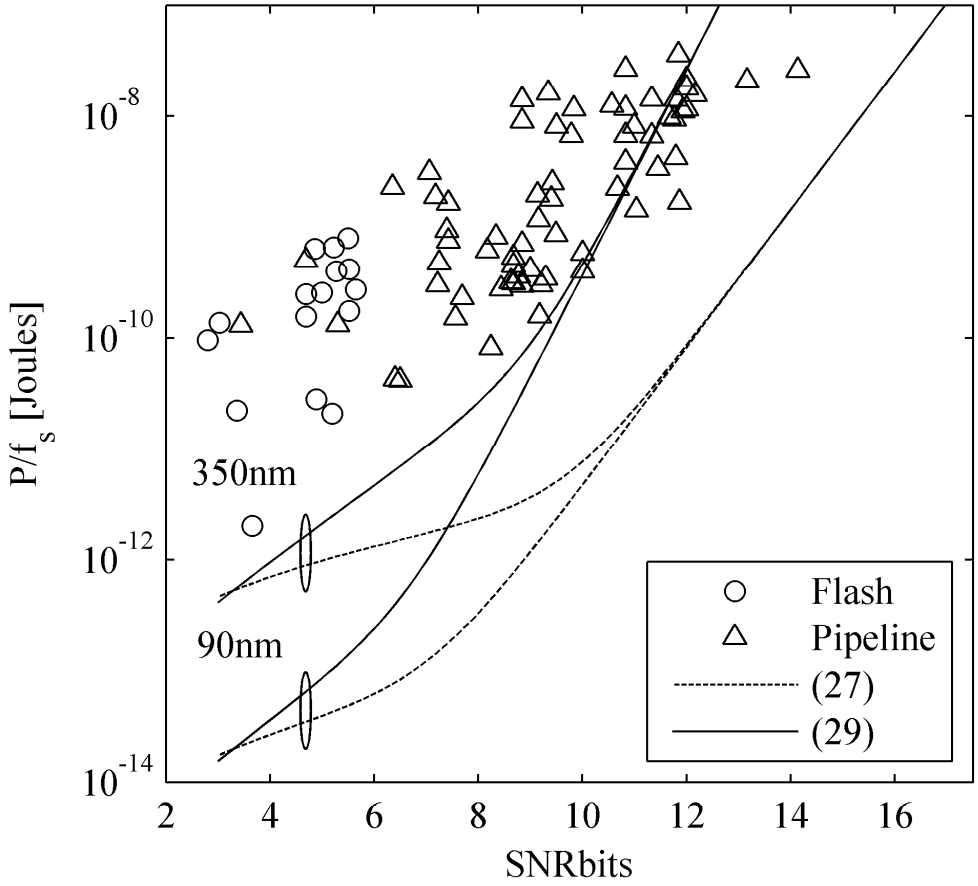
Matching may require large C - increased power

Linearity may require smaller V_{FS} – increased power

RF circuits can utilize passive matching – may decrease power

Power amplifiers need other goals – high efficiency

Applications: ADC



Plot of minimum ADC power for two processes

"(27)" this theory pipelined ADC
"(29)", theory flash ADC

Two processes, 90nm and 350nm (V_{dd}=1V, V_{eff}=100mV, C_{min}=1fF, V_{dd}=3V, V_{eff}=300mV, C_{min}=3fF)

Triangles, experimental pipelined
Circles, experimental flash

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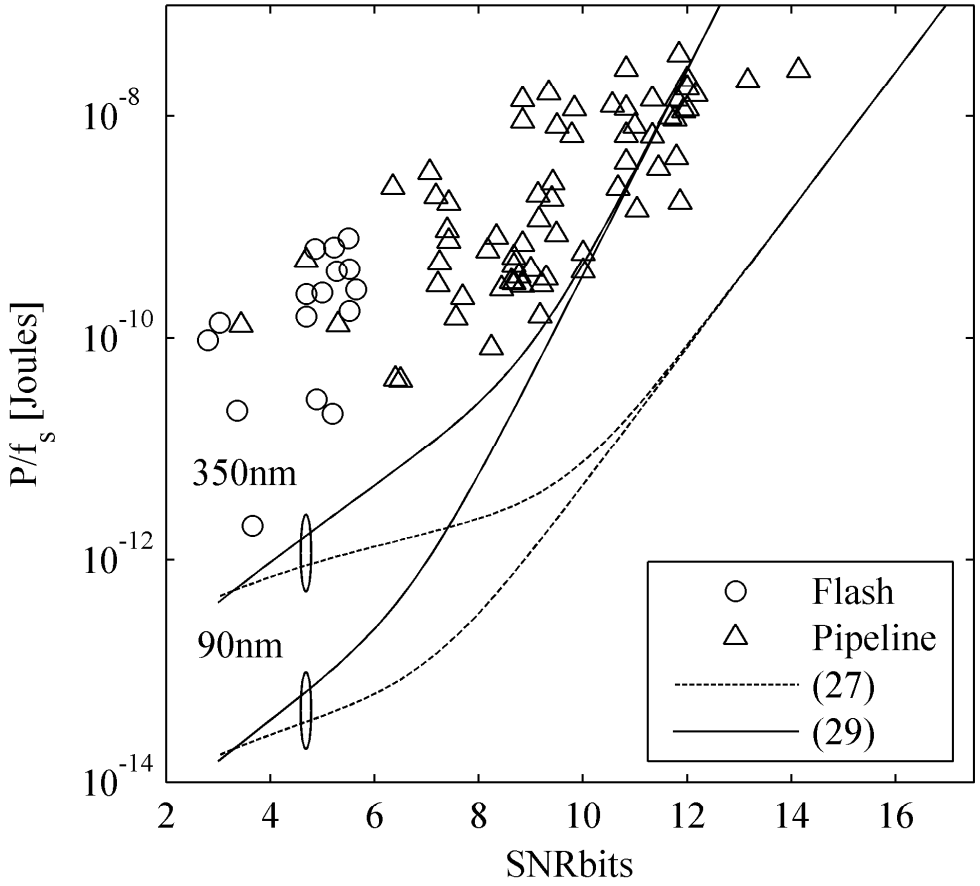
Applications: ADC



Note1:

High resolution, noise limited
Low resolution, process limited

Note2:

High resolution, experimental approaches theory (10x difference)

Low resolution, larger discrepance (larger development potential)

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Conclusions

Power consumption in analog parts can be addressed

Smart choices of architecture, circuit topology, and parameters can save power

For large dynamic range, digital often use less power
More so in scaled technologies
Move functions to digital
Perform digital correction of analog parts to save analog power

References

E.A. Vittoz, “Future of Analog in the VLSI Environment”, Proc. ISCAS´90, p. 1372-1375, 1990.

E. A. Vittoz, “Low Power Design: Ways to Approach the Limits”, ISSCC 1994, Digest of technical papers, p. 14-18, 1994.

C. C. Enz and E. A. Vittoz, “CMOS Low-Power Analog Circuit Design”, in Designing Low Power Digital Systems, Emerging Technologies, p 79-133, Atlanta 1996.

A.-J. Annema, B. Nauta, R. van Langevelde and H. Tuinhout, “Analog Circuits in Ultra-Deep-Submicron CMOS”, JSSC, vol. 40, p. 132-143, January 2005.

T. Sundström, B. Murmann and C. Svensson, “Power Dissipation Bounds for High-Speed Nyquist Analog-to-Digital Converters”, IEEE Trans. Circuits ad Systems, vol. 56, pp. 509-518, March 2009.

C. Svensson and J. Wikner, “Power consumption of analog circuits: a tutorial”, Analog Integrated Circuits and Signal processing, vol. 65, issue 2, pp. 171-184, October 2010.