2.7 Assume that the power supply voltage is V_{DD1} = 5 V. The power consumption for the one-PE solution is:

$$P_1 = C f V_{DD1}^2$$

where C is the equivalent switched load and f is the switch frequency. Now, using two PEs, the available computation time for each PE is doubled. Hence, the switch frequency can be halved. Assume that the load for each PE increases to $1.1C$ due to the larger circuit area and additional wire routing. The propagation delay may be doubled, hence the power supply voltage can be reduced to

$$\frac{t_{p2}}{t_{p1}} = \frac{\frac{1.1\ CV_{DD2}}{(V_{DD2} - V_T)^2}}{\frac{CV_{DD1}}{(V_{DD1} - V_T)^2}} = \frac{1.1\ V_{DD2}(V_{DD1} - V_T)^2}{V_{DD1}(V_{DD2} - V_T)^2} = \frac{1.1\ V_{DD2}(5 - 0.75)^2}{5(V_{DD2} - 0.75)^2} = 2$$

Solving for V_{DD2} we get

$$19.869\ V_{DD2} = 10(V_{DD2}^2 - 1.5\ V_{DD2} + 0.5625)$$

and $V_{DD2}^2 - 0.486875\ V_{DD2} - 0.5625 = 0$

V_{DD2} = 0.16957 V or 3.3173 V Hence, V_{DD2} = 3.3173 V since the supply voltage must be larger than V_T. The power consumption can be reduced to

$$P_2 = 2.2C\ \frac{f}{2}\ V_{DD2}^2 = 2.2\ \frac{1}{2}\frac{V_{DD2}^2}{V_{DD1}^2}\ C f V_{DD1}^2 = 1.1\ \frac{3.3173^2}{5^2}\ P_1$$

$$P_2 = 0.484\ P_1$$

Conclusion: It is necessary to reduce the supply voltage when geometry's are scaled down. This reduces the power consumption, but also the speed. Now, the reduction in minimum feature size increases the speed and the number of devices that can be put onto a single chip. Thus, the expected increase in speed will not be as large as was expected from the simple scaling policy that was discussed in section 2.6. It is therefore advantageous to use highly parallel algorithms that can exploit the large number of devices that can be put onto the chip in order to achieve high throughput implementations.