8.6 Assume that the area scales quadratically which is somewhat pesimistic since the number of metal layers are increased in modern processes. TMS320C25 is manufactured in a 1.8 μm CMOS technology and with a clock frequency of 50 MHz. If the 0.35 μm technology is used, the area can be reduced to $\frac{(0.35)^2}{(1.8)^2} = 0.04$, or to about 4% of the original area.

The clock frequency can be estimated according to equation (2.6). The 1.8 μm process has a threshold voltage in the range 0.8~0.9V and the 0.35 μm has a threshold voltage in the range 0.5~0.6V. We take $V_{T_{1.8\mu m}} = 0.8\,\text{V}$ and $V_{T_{0.35\mu m}} = 0.5\,\text{V}$, the maximum clock frequency can be estimated by

$$f_{0.35\mu m} \approx \frac{(V_{DD_{0.35\mu m}} - V_{T_{0.35\mu m}})^{1.55}}{(V_{DD_{1.8\mu m}} - V_{T_{1.8\mu m}})^{1.55}} \cdot \frac{V_{DD_{1.8\mu m}}}{V_{DD_{0.35\mu m}}} \frac{C_{L_{1.8\mu m}}}{C_{L_{0.35\mu m}}} \cdot f_{1.8\mu m}$$

$$\approx \frac{(3.3 - 0.5)^{1.55}}{(5 - 0.8)^{1.55}} \cdot \frac{5}{3.3} \cdot \left(\frac{1.8}{0.35}\right)^2 \cdot 50 \times 10^6 \approx 1 \times 10^9 (\text{Hz})$$

However, there are many other problems in designing such high frequency processors, like clock skew and power supply, etc. The most DSP processor are running at 100 MHz to 200 MHz currently while general purpose processors are running at 500 to 800 MHz.