Linear CMOS-PA design in different 28 nm technologies

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Introduction and Outline

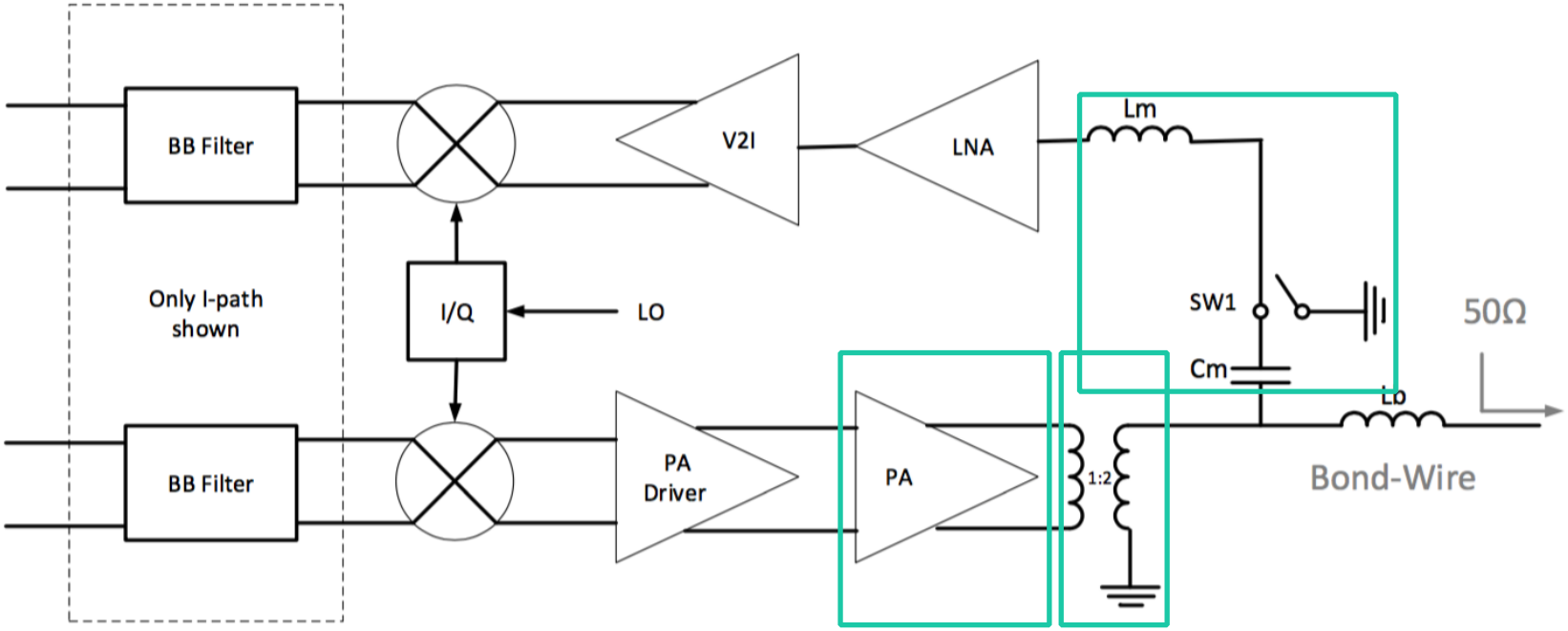
- Prestudy project within Smartare Elektroniksystem:
  - Linear PA design for WLAN 802.11ac (EVM)
  - f=5 GHz, BW=80 MHz, modulation=256QAM
  - PA comparison: 28 nm bulk and FD-SOI technology
  - PA reliability

- A 28 nm bulk CMOS PA design for 802.11ac
- A 28 nm FD-SOI high-power stacked PA core (on-going)
- Reliability for 28 nm CMOS-PAs

A 28 nm CMOS PA design for 802.11ac

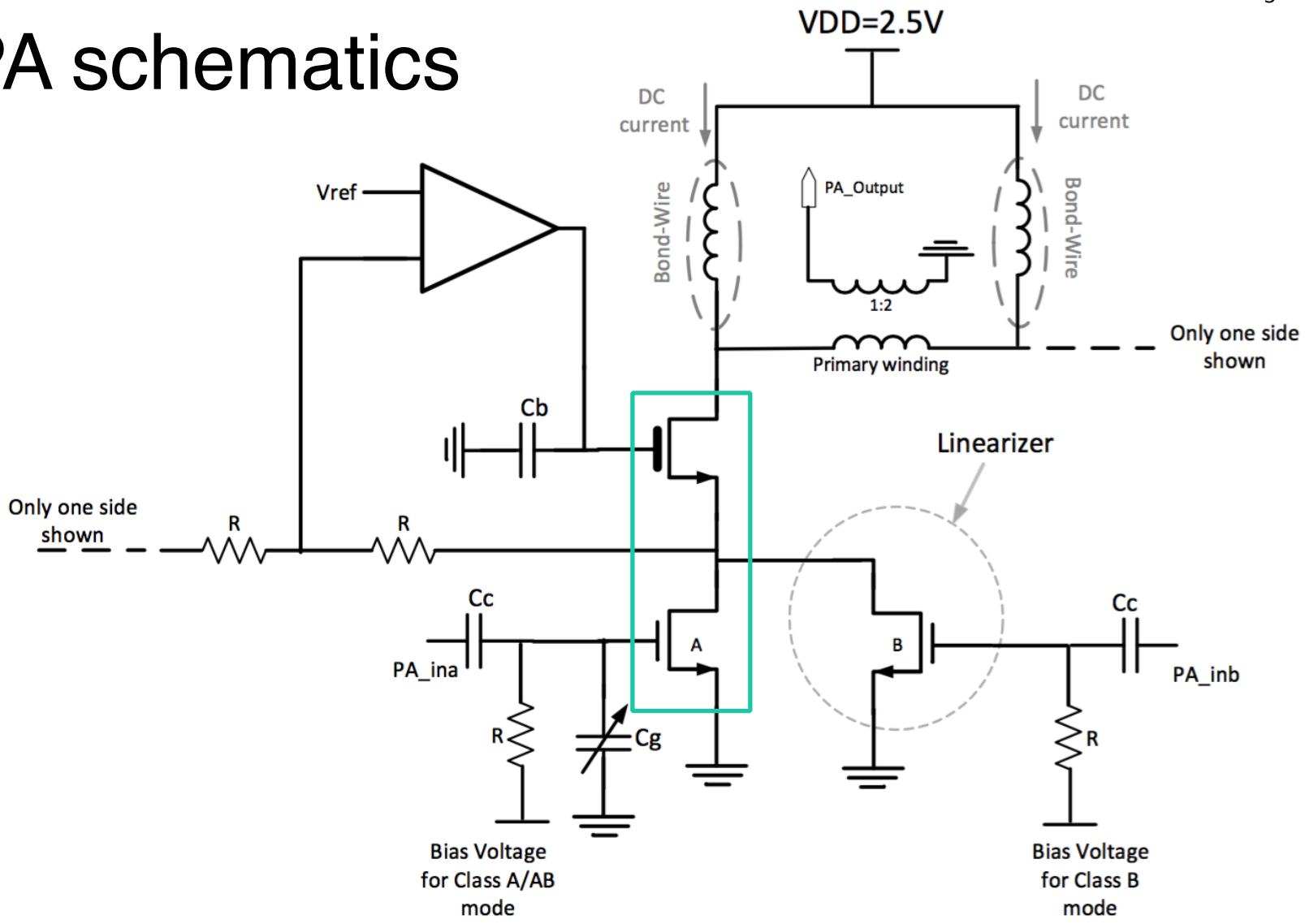
- Class AB PA
- Integrated balun and integrated Tx/Rx switch
- 802.11ac 5 GHz band
- 28 nm bulk CMOS
- Circuit solutions to improve the linearity of the PA and reduce memory effects
- No external components
- No linearization using predistortion (DPD)

Transceiver architecture



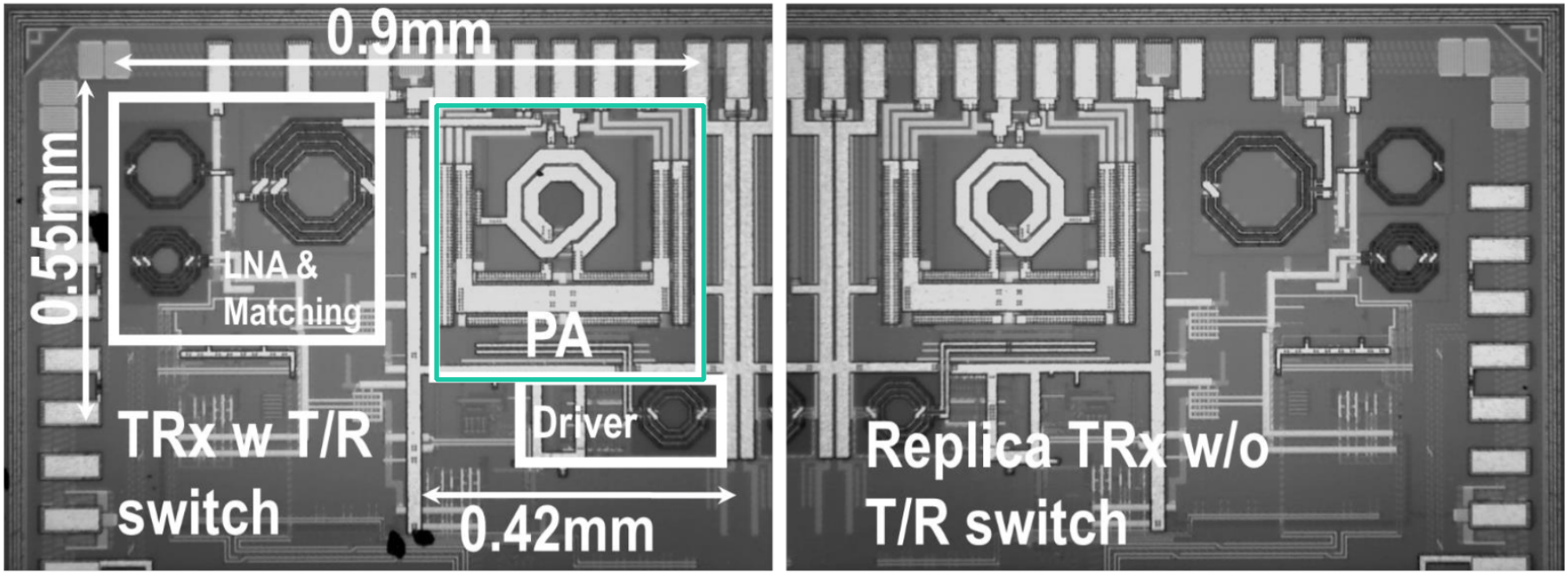
Including PA, balun and Tx/Rx Switch. Also LAN for Rx.

PA schematics



A 28 nm CMOS PA design for 802.11ac

- Die micrograph showing PA, LNA and T/R Switch.

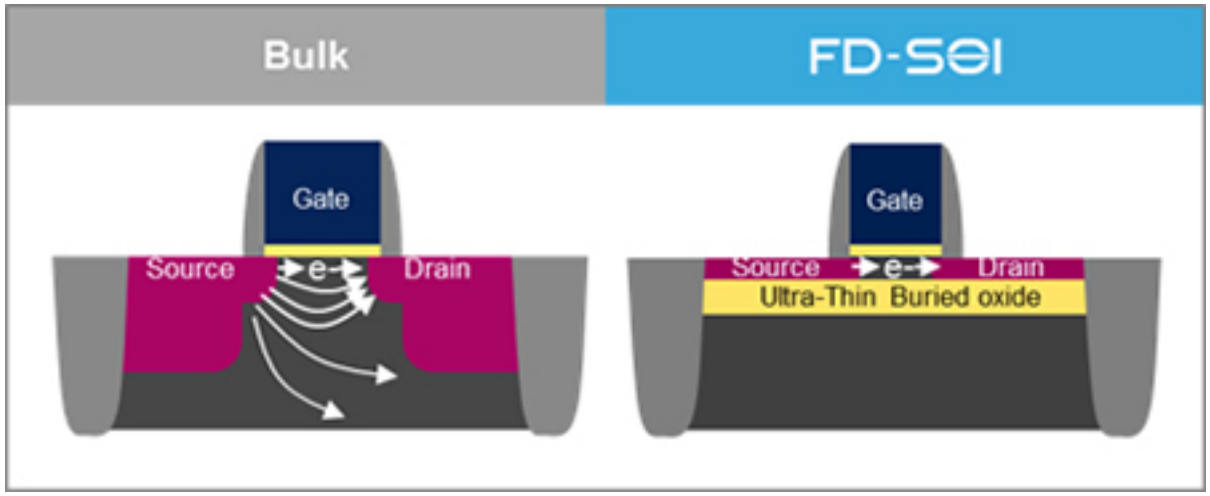


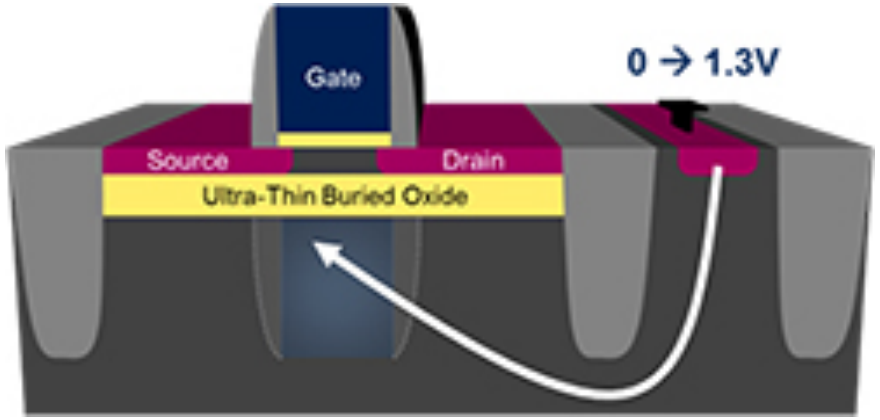
Performance and comparison table

	This work	Ref. [2] ISSCC 2015	Ref. [5] ISSCC 2014	Ref. [4] RFIC 2014
External components	NO	N/A	N/A	N/A
Integrated Tx/Rx Switch	Yes	NO	NO	Yes
Frequency (GHz)	5.0 - 5.8	2.0 - 6.0	5(5)	5(8)
Psat (dBm)	23.5	20.5(3)	N/A	26
Efficiency %	22	20	N/A	N/A
RF Power Consumption	530mW(1)	N/A	1520mW(6)	1722mW(9)
Output Power @ -32dB EVM 802.11ac VHT80 MCS9	13 dBm	7dBm(4)	3	17.5dBm(10)
DPD	NO	NO	NO	Yes
Technology	28nm	65nm	40nm	55nm
PA + T/R switch Die Area/RF+BB filters (mm2)	0.7x0.4/0.9x1.3(2)	0.57x1.57	21.5(7)	7.7(11)

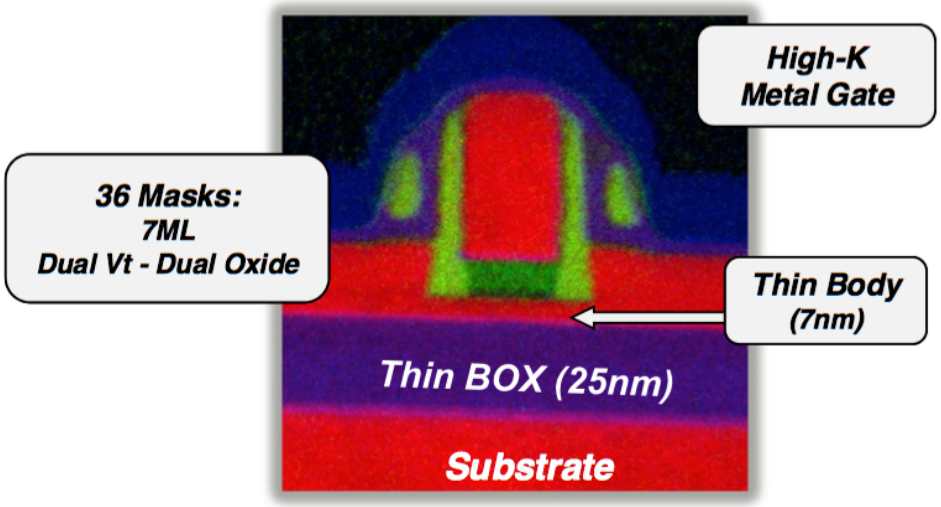
(1) PA & driver power consumption,VHT80, MCS9 @ 13dBm
(2) Area without synthesizer
(3) Psat @5.5GHz
(4) Output power from 5 - to - 6GHZ
(5) Reported -32dB EVM only @5.7GHz
(6) SOC power consumption, MIMO, 3ss, VHT80 @ -5dBm
(7) Radio + Analog (including data converter and pads)
(8) Reported -32dB EVM only @5.8GHz
(9) RF power consumption, MIMO, 2ss ,VHT40 @ 17.5dBm
(10) The output power reported is including Digital Pre Distortion
(11) WiFi RF + Analog

UTBB vs. bulk CMOS





28 nm FD-SOI (STM)

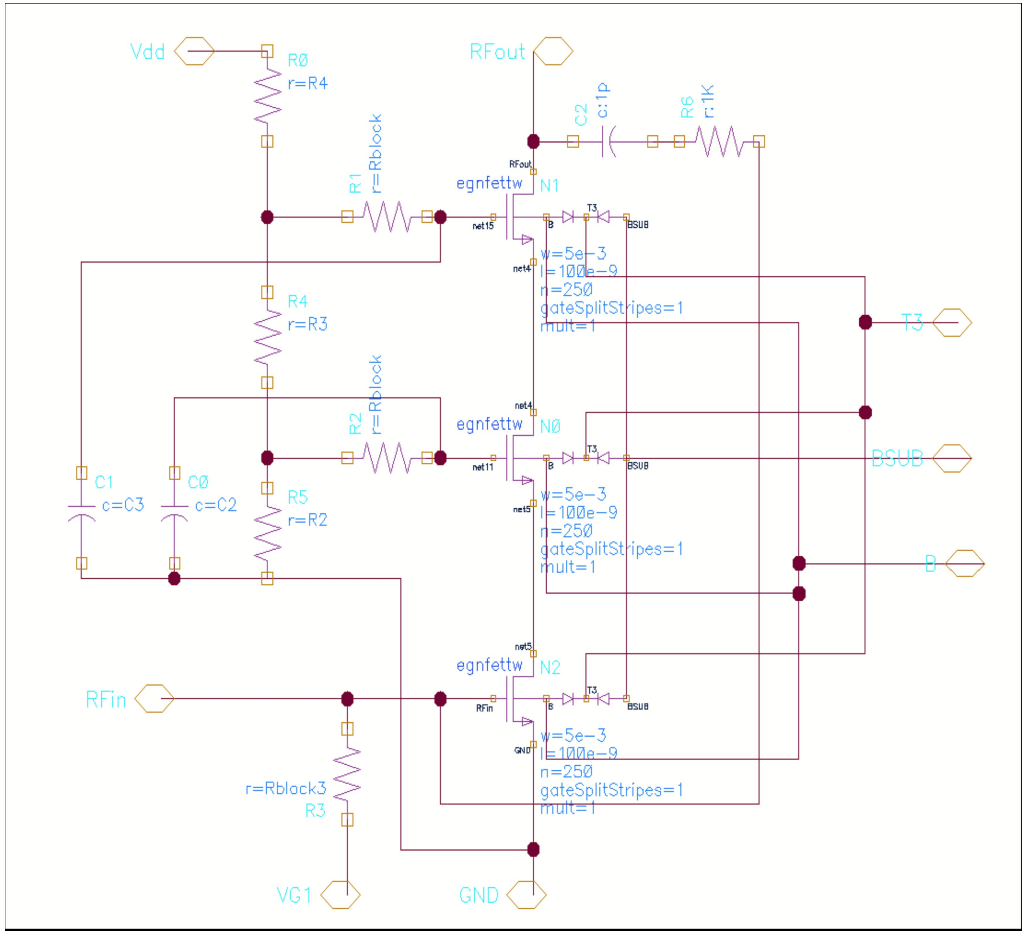


L_g=24 nm, T_{ox}=1.8 nm, V_{sup}=1.0 V
ultra-thin silicon: 7 nm
ultra-thin buried oxide: 25 nm

High-k dielectric
Metal-gate electrode
S/D: epitaxy raised
Undoped channel
Bulk/SOI integration

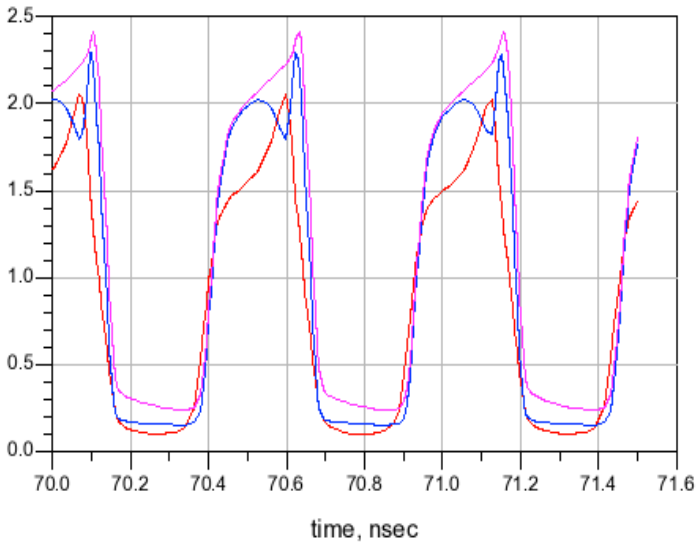
PA design:
L_g=150 nm, T_{ox}=2.8 nm,
V_{sup}=1.8 V (+10 %)

3-stacked PA core for high power using SOI



*W = 6000 um (10 um * 10 * 60 cells)*
Vdd=3.0 V
Class-AB
f=1900 MHz
*Zin = 0.49 + j*7.1 Ω*
RL=7 Ohm
C2=4 pF, C3=1 pF

P-1dB= 28.9 dBm



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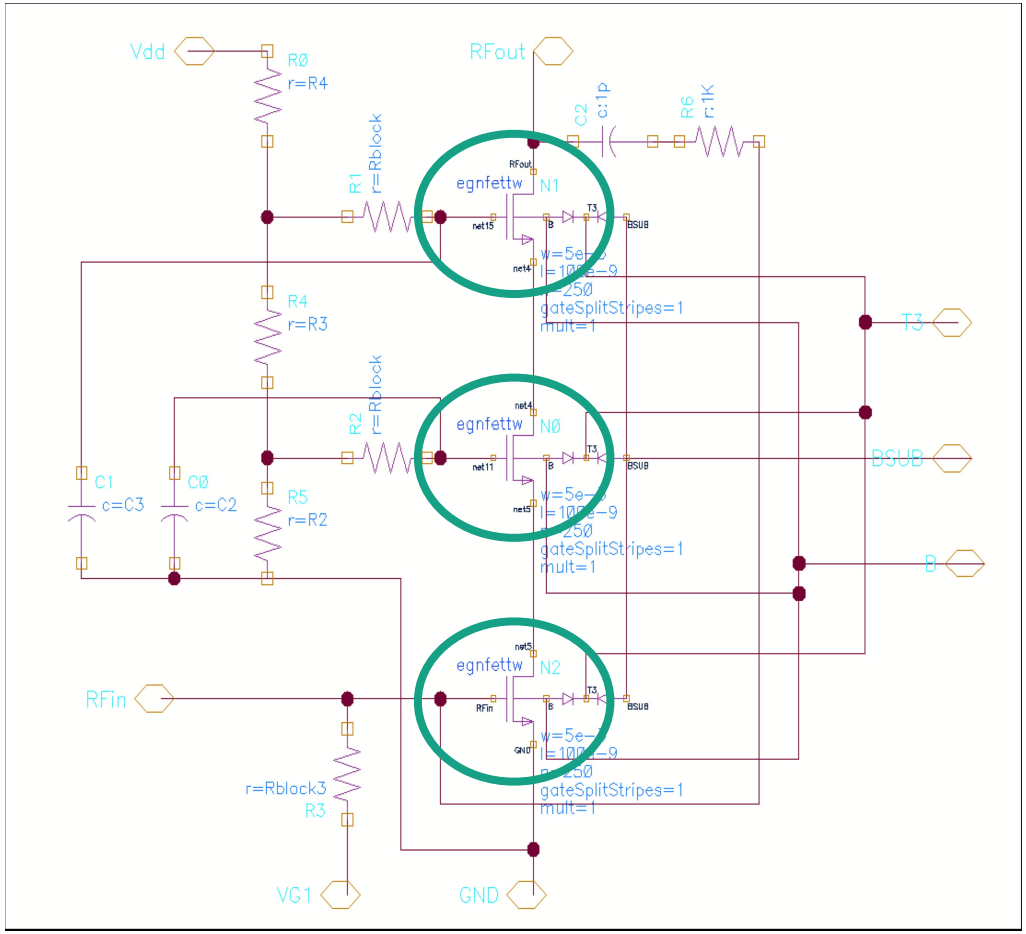

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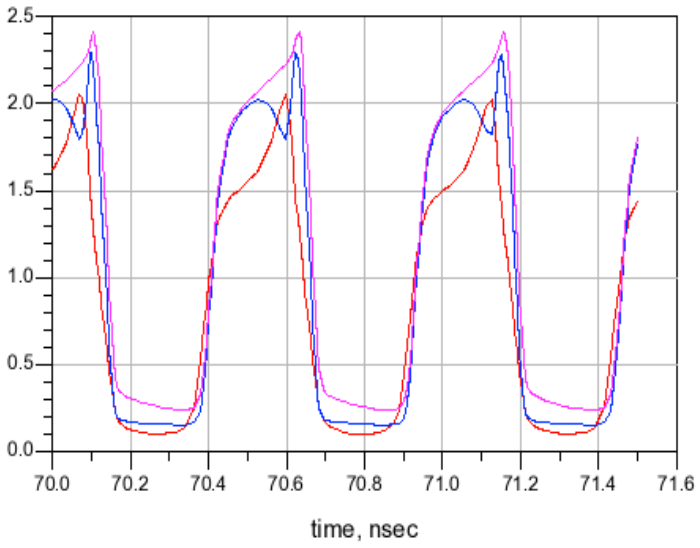

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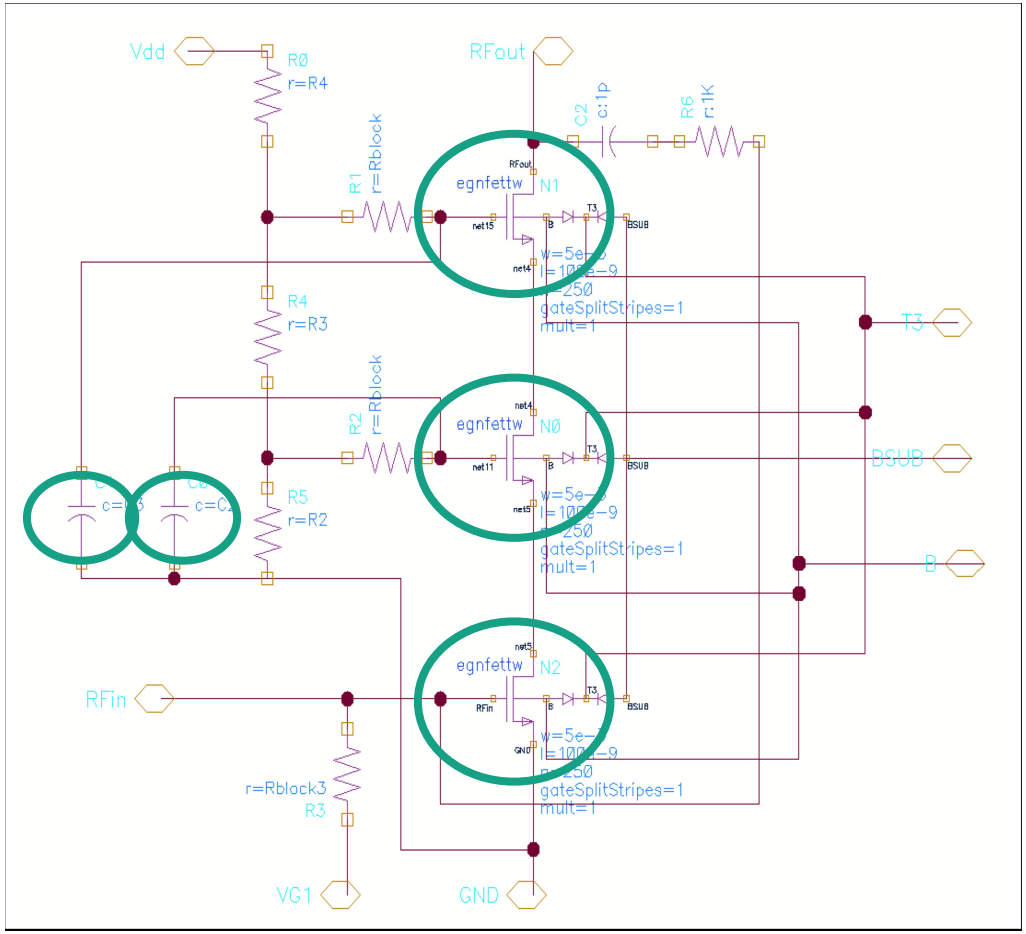

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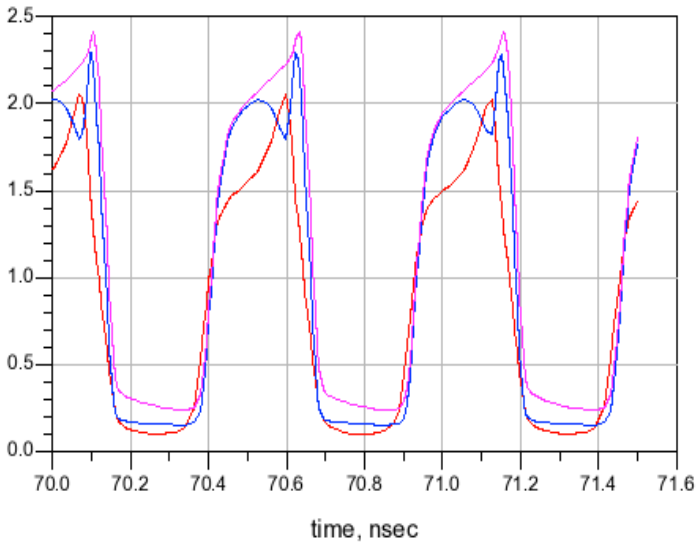
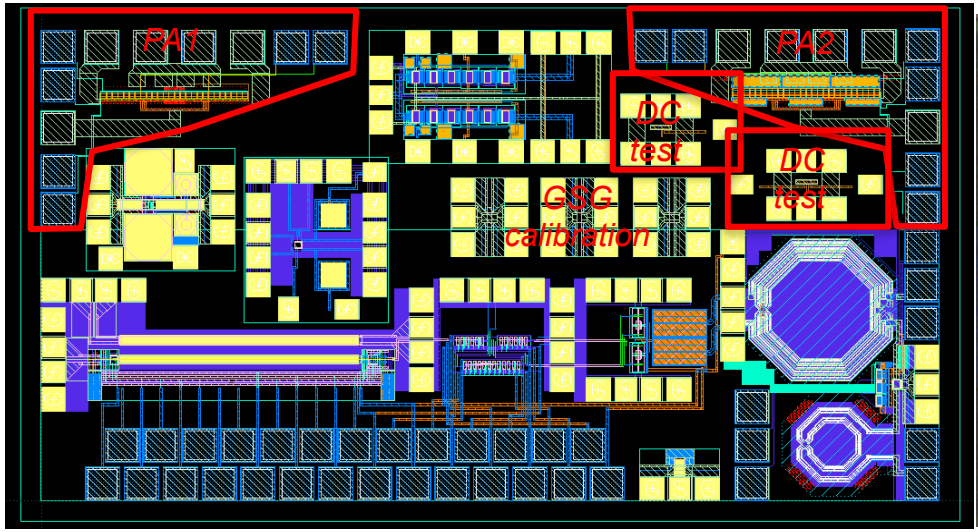
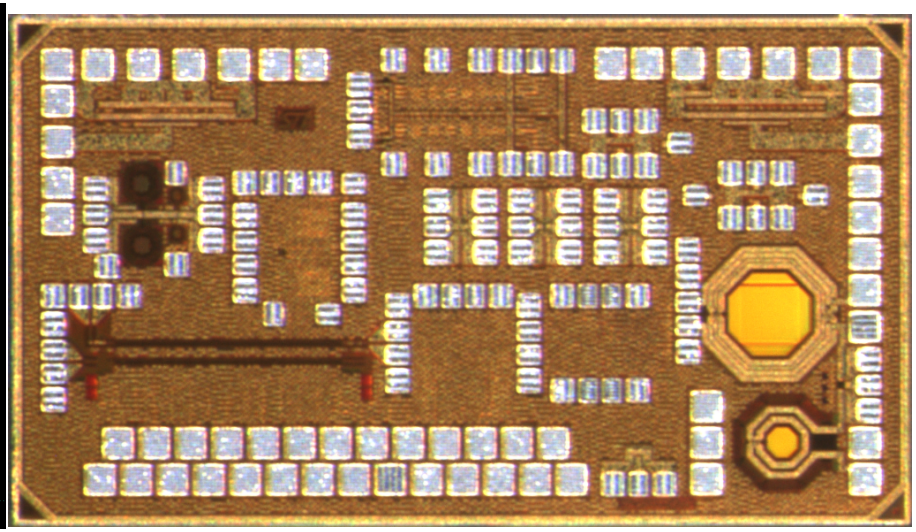


3-stacked PA for high power using SOI

- Designed with Acreo Swedish ICT
- Test chip = 1.5 x 2.2 mm^2
- PA, LNA, antenna switch, RX chain, mixer
- PA under evaluations





CMOS PA reliability

- Class AB PA experiences up to 2x V_{DD} on output node.
- Stress cases not covered by design manuals.
- HKMG gate material ($SiO(N)/HfO_2$).

- Reliability estimations:
  - Estimation of peak ”duty cycle” (e.g. >90 % of max voltage).
  - ”Use Cases” to translate to product lifetimes
    => usually translates to 100-500 h effective @ high stress.
  - Lab measurements: PA at CW and elevated supply, RF performance degradation checked regularly:
    no performance degradation.

Summary and Conclusions

- Bulk CMOS will be the preferred choice for future products.
- Need to better understand EVM and increase P_{sat} to generate higher linear P_{out}.
- Add DPD to further improve the linearity.
- Increased efficiency => new PA architecture needed.
- Stacked PA design in SOI interesting to further increase output power and use higher voltages, but tricky design solutions.
- CMOS PA reliability necessary to understand and verify.

Funded by the Strategic Innovation Program
"**Smartare Elektroniksystem**",
a joint venture of the
Swedish Governmental Agency for Innovation Systems,
the Swedish Research Council Formas,
and the Swedish Energy Agency