The 28 nm CMOS Power Amplifier

IECC 2017

Keynote talk 2017-05-19

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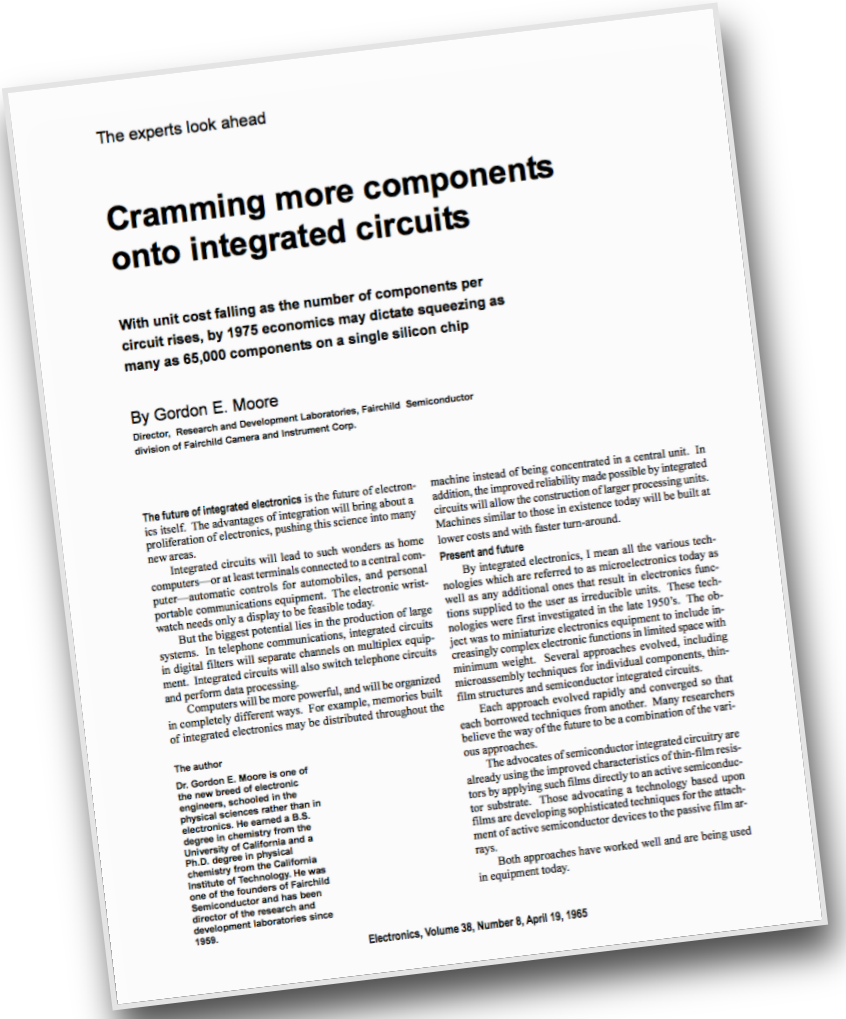
Outline

- Moore's law
- Dennard scaling
- CMOS scaling beyond 130 nm

- Moore's law and radio circuit design
- The 28 nm CMOS Power Amplifier (PA)
- PA design in scaled CMOS for wireless applications
- FinFET and radio design

Moore's law is not about scaling but economy!



The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore
Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.

Present and future

By integrated electronics, I mean all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as irreducible units. These technologies were first investigated in the late 1950's. The object was to miniaturize electronics equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including microassembly techniques for individual components, thin-film structures and semiconductor integrated circuits.

Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the way of the future to be a combination of the various approaches.

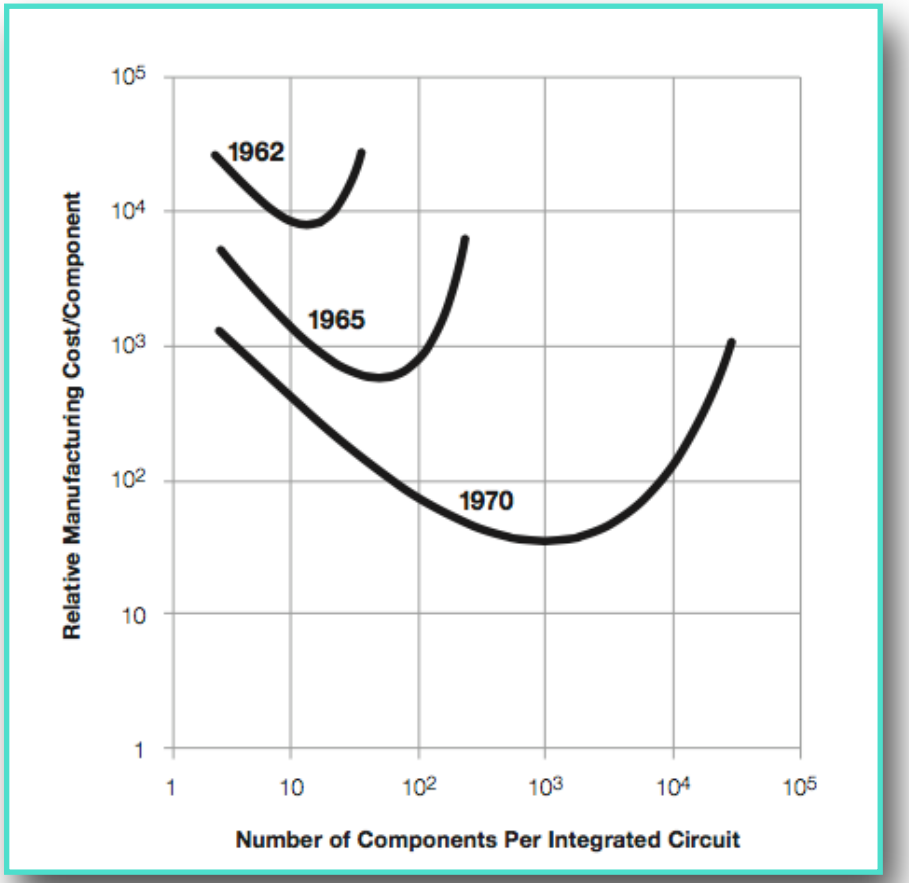
The advocates of semiconductor integrated circuitry are already using the improved characteristics of thin-film resistors by applying such films directly to an active semiconductor substrate. Those advocating a technology based upon films are developing sophisticated techniques for the attachment of active semiconductor devices to the passive film arrays.

Both approaches have worked well and are being used in equipment today.

The author

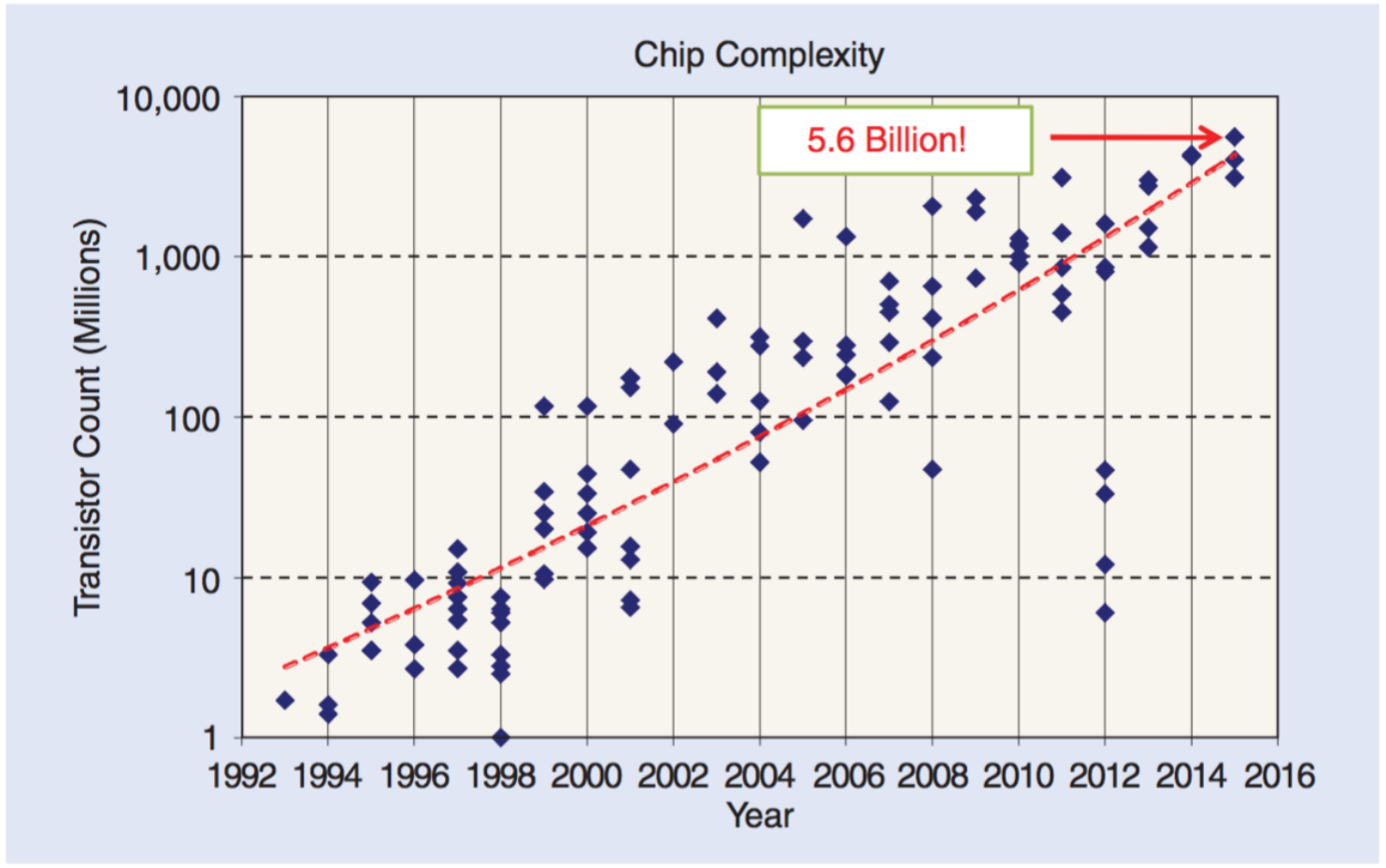
Dr. Gordon E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1959.

Electronics, Volume 38, Number 8, April 19, 1965



G. E. Moore, Electronics 1965

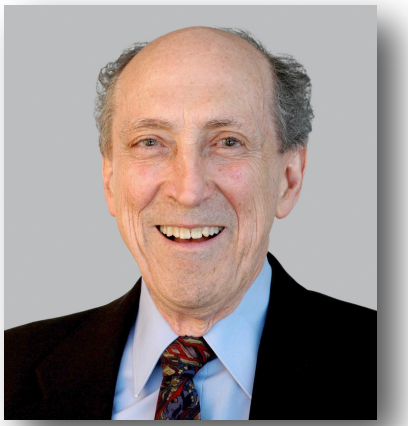
Number of transistorer per chip



ISSCC 1970-2015:
Doubling each 24 month

Dennard scaling of MOS devices

Component/circuit parameter	Scaling factor*
Component dimension/thickness	$1/\lambda$
Doping concentration	λ
Gate oxide thickness	$1/\lambda$
Supply voltage	$1/\lambda$
Current	$1/\lambda$
Capacitance	$1/\lambda$
Delay time (1/speed)	$1/\lambda$
Transistor power	$1/\lambda^2$
Energy efficiency (”MIPS/W”)	$1/\lambda^3$
Power density	1



Robert Dennard

* constant electrical field

Dennard et al., JSSC, pp. 256-268, Oct 1974
Dennard, SSC Mag, pp. 29-38, No. 2, 2015

Dennard & Moore 1975-2000: The winning team!

Dennard scaling when transistors getting smaller:

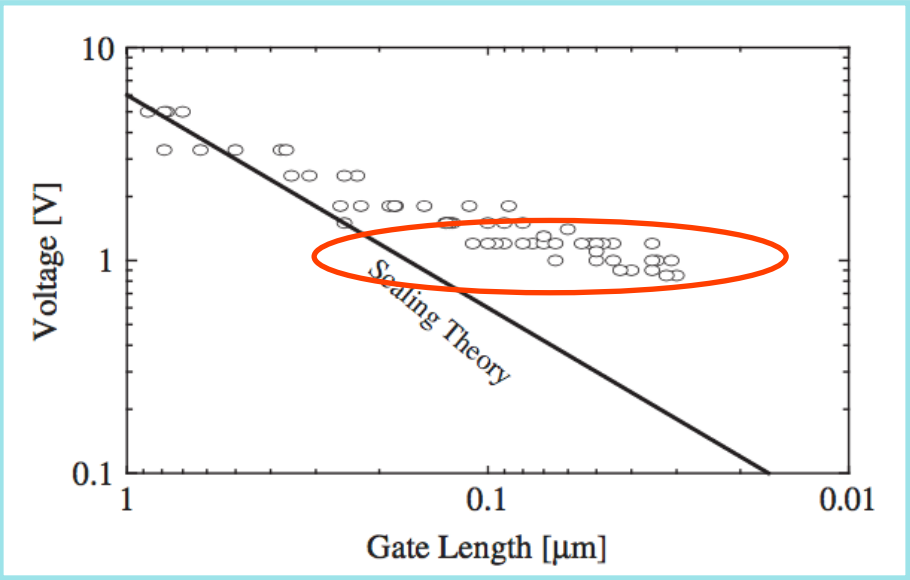
- faster components and circuits,
- lower total power (constant power density),
- electronics can be made smaller, lighter, faster, better.

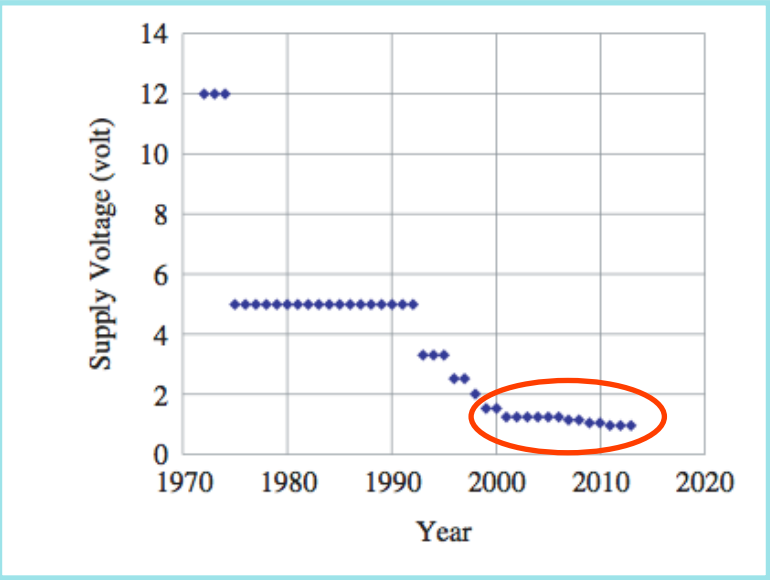
Moore's law:

- same cost per area when components scale,
- more transistors per chip,
- lower cost per transistor.

Problem with Dennard scaling

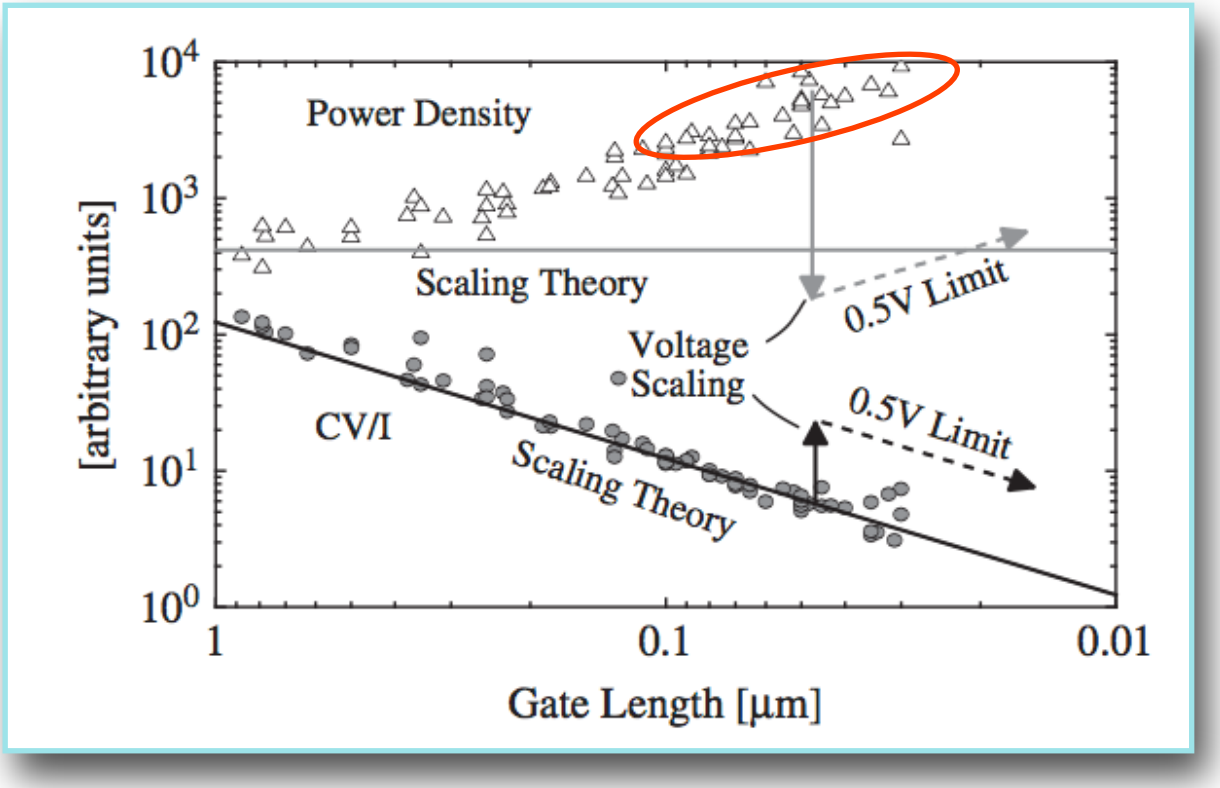
- Supply voltage was not properly scaled, more like 1/sqrt(λ).
- Supply voltage reduction in practice stopped more than ten years ago.
  - Thermal noise (kT/q = 25 mV at room temperature),
  - Sub-threshold leakage (power consumption, thermal issues).



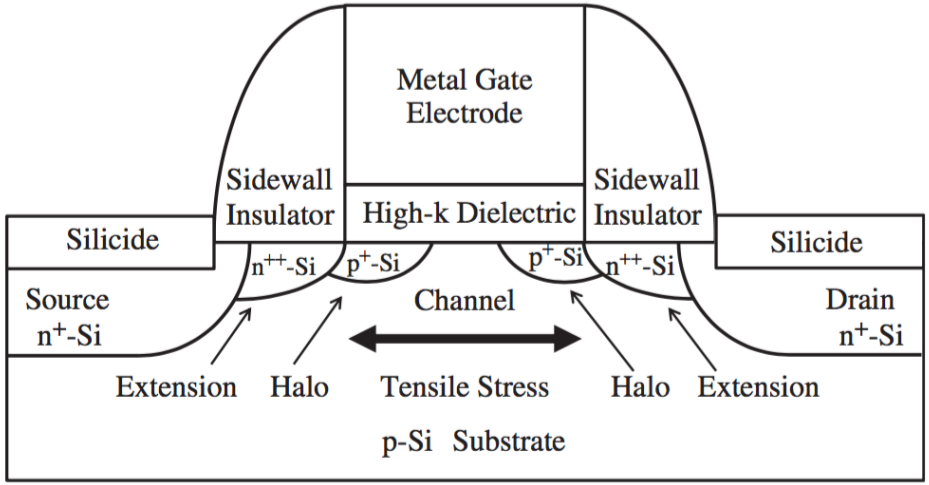


Problem with Dennard scaling

- Power consumption limits the scaling
- Increased clock speed leads to higher power consumption



CMOS scaling down to 130 nm was rather ”linear”



32/28 nm bulk MOSFET

90 nm: mechanical strain in the channel => higher mobility

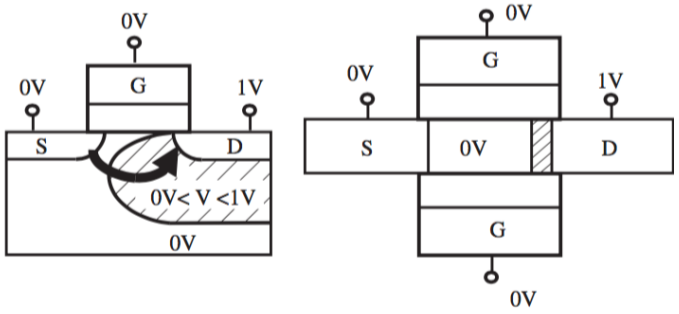
90 nm: PD-SOI (reduced switching time, corresponding to one process node, but more higher substrate cost).

45 nm: Material with higher dielectric constants replacing SiO_2 as insulator in the gate (reduced leakage currents)

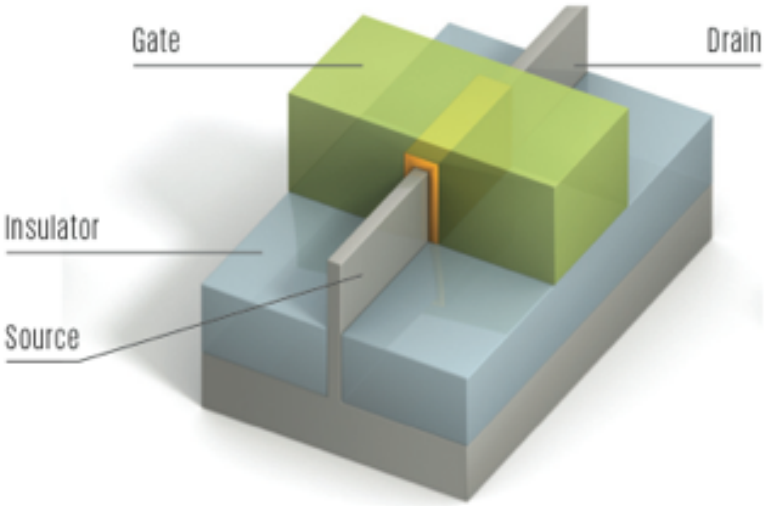
28 nm: Metal gate (smaller threshold voltage variations)

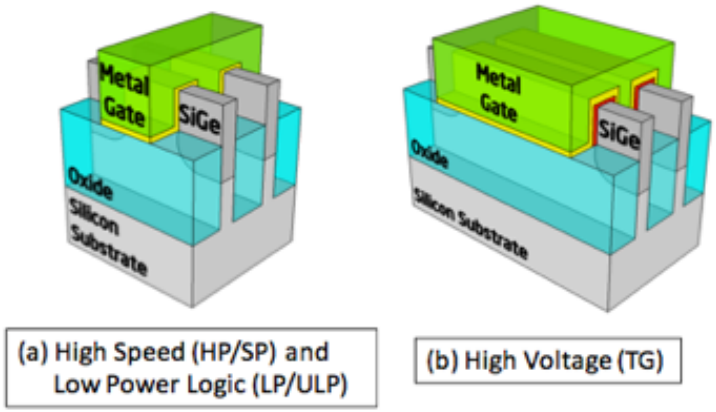
28 nm: FD-SOI
Thin undoped channel with device properties given by vertical dimensions and backside bias.

22 nm: Tri-Gate or FinFET



FINFET ADVANTAGES	
PARAMETER	**DETAILS**
Power	Much lower power consumption allows high integration levels. Early adopters reported 150% improvements.
Operating voltage	FinFETs operate at a lower voltage as a result of their lower threshold voltage.
Feature sizes	Possible to pass through the 20nm barrier previously thought as an end point.
Static leakage current	Typically reduced by up to 90%
Operating speed	Often in excess of 30% faster than the non-FinFET versions.





Intel 22 nm with extensions for SoC design (Jan et al., IEDM 2012)

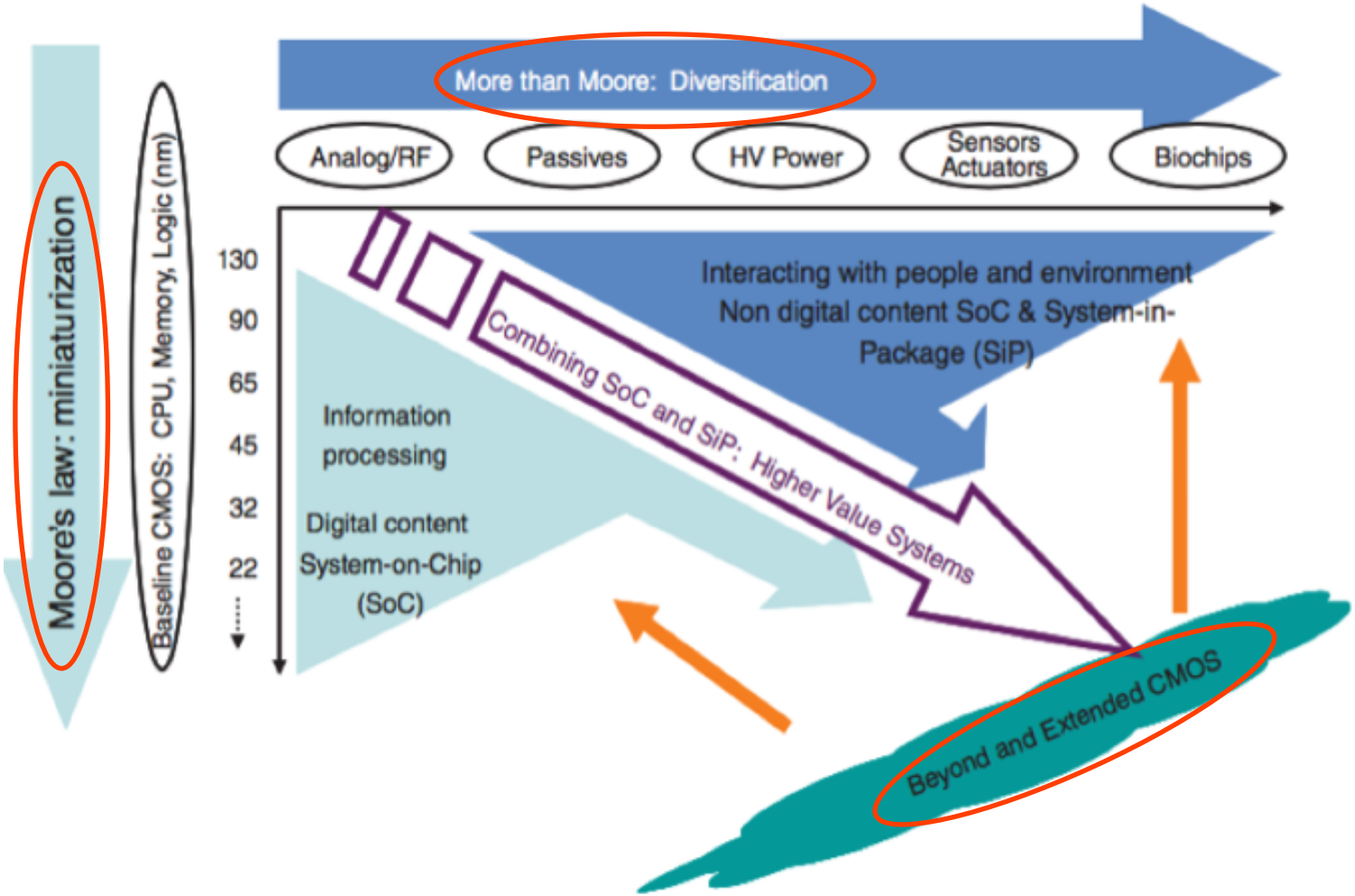
First description? Hisamoto et al., TED 1991

2017: State-of-the-art is 10 nm

- Early 2015: Intel says 10 nm delayed until 2017 (ITRS=2015)
- April 2015: TSMC announced that 10 nm production would begin at the end of 2016.
- May 2015: Samsung Electronics showed off a 300 mm wafer of 10 nm FinFET chips.
- August 2016: Intel began trial production at 10 nm.
- October 2016: Samsung Electronics announced mass production at 10 nm.
- April 2017: Samsung started shipping their Galaxy S8 which uses Samsung's version of a 10 nm processor.

Wikipedia

Moore's law in several dimensions



Moore's law and radio circuit design

- Nodes for many new radio circuit designs today is 28 nm on bulk substrate or FD-SOI. 40 and 55 nm also popular.
- Nodes give more than fast enough transistors for all wireless communication in the 1-6 GHz bands (mobile comm, wireless networks, sensors, etc.), but also for short range communication (e.g. 5G, 28 - 60 - 100+ GHz).
- Demands for high level of integration (of digital blocks) make the selected processes less suitable for radio design - too small nodes - but we still have to live with this problem!

The power amplifier (PA)

- Last active part in the transmitter before the antenna. Boosts the signal to higher power levels for transmitting the signal to a distant receiver.
- Power levels:
  - Cellular phones: 23-24 Bm (Pav), up to 30 dBm (Ppeak),
  - WLAN: up to 20-23 dBm (Pav), up to 30 dBm (Ppeak),
  - Bluetooth: typically around 5 dBm.
- Frequency range often in the 1-6 GHz interval for CMOS integrated PAs

The power amplifier (PA)

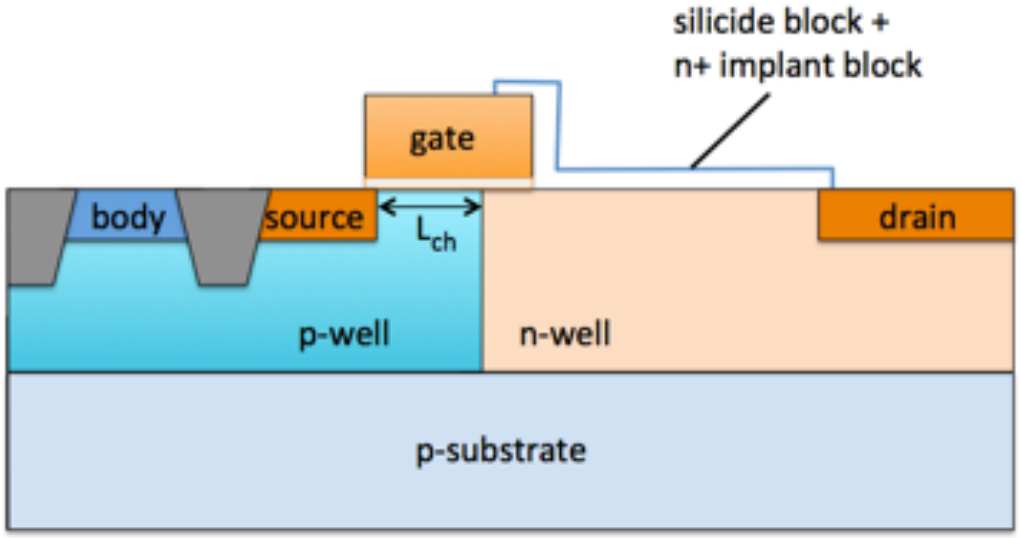
- Requirements for portable applications (consumer-oriented):
  - high integration => low price,
  - battery operation => high efficiency needed,
  - high linearity => high data rate.

How to reach high PA output power

- Large devices (many parallel transistors) + impedance transformation. Power combination using (on-chip) transformers.
- High supply voltage $$P = \frac{V^2}{2R}$$
- ”Digital” PAs (class-D inverter-based, using normal supply voltage)

How to handle the high supply voltage?

New component/new structures



LDMOS structure with no additional process steps or masks*

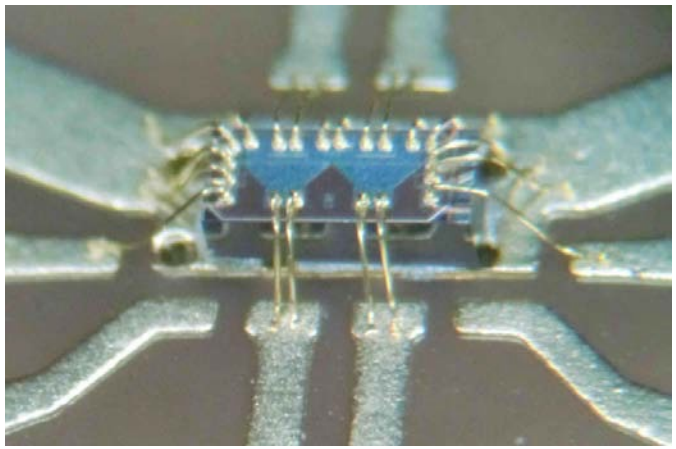
Designed in Global Foundry's 65 nm CMOS-process for WLAN applications.
Concept scalable to (available in) 45 nm and 32/28 nm.

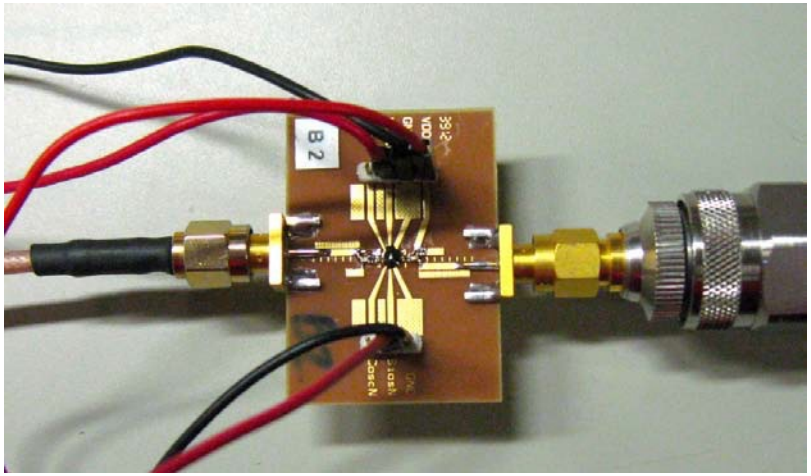
T. Johansson et al., EuMIC 2013

T. Johansson et al., EuMIC 2013

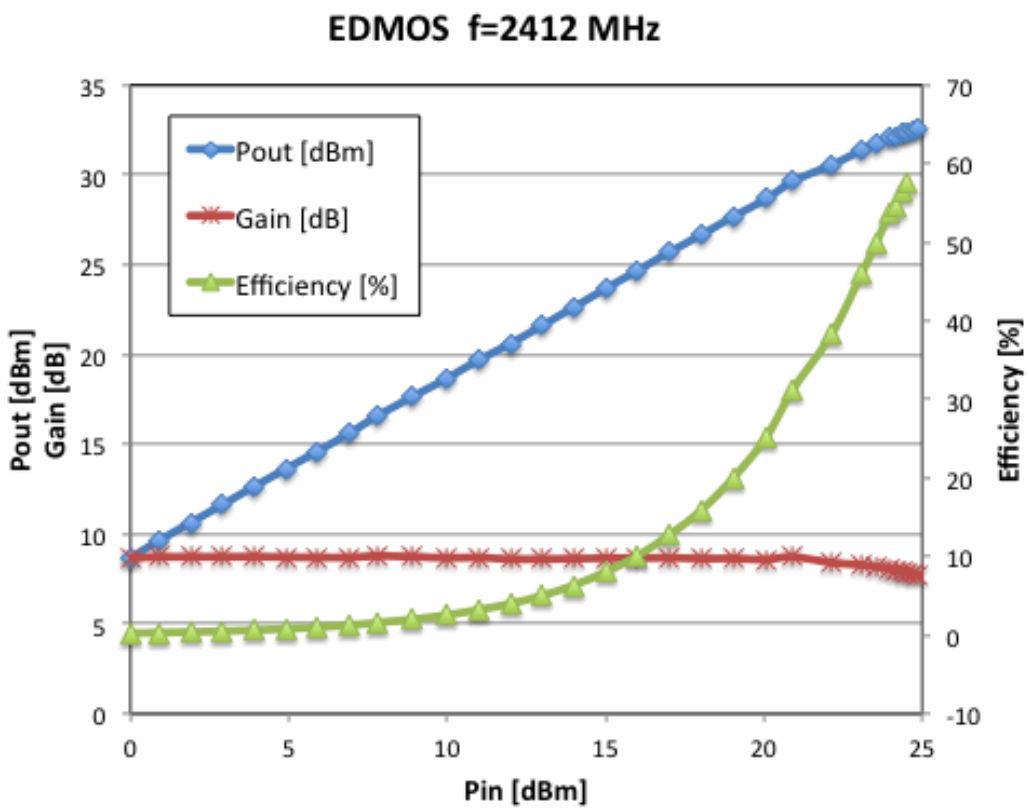
WLAN PA

- Transistors with W=5.6 mm mounted on PCB



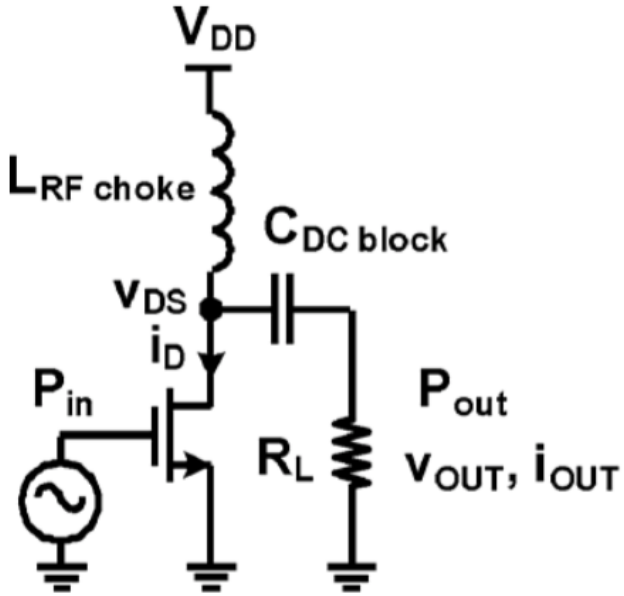


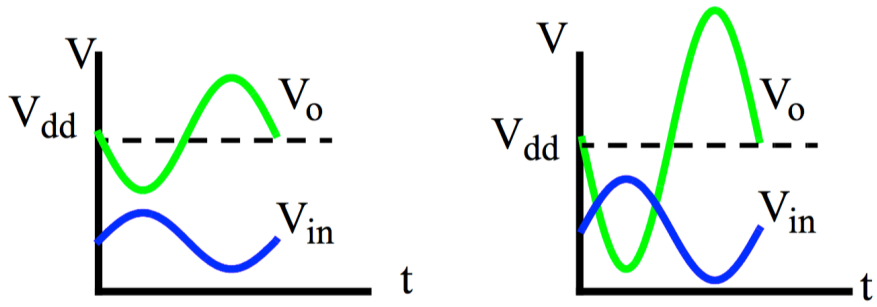
Differential PA, Vdd=3 V, f=2412 MHz
P-1dB = 32,5 dBm (1,8 W).
Class AB, efficiency over 50 % for unmodulated signal.



The linear PA

- Linear PAs (class A, AB, …) are the most commonly used amplifier classes on radio PA design.
- Drawback: 2 x supply over the drain node of the transistor.

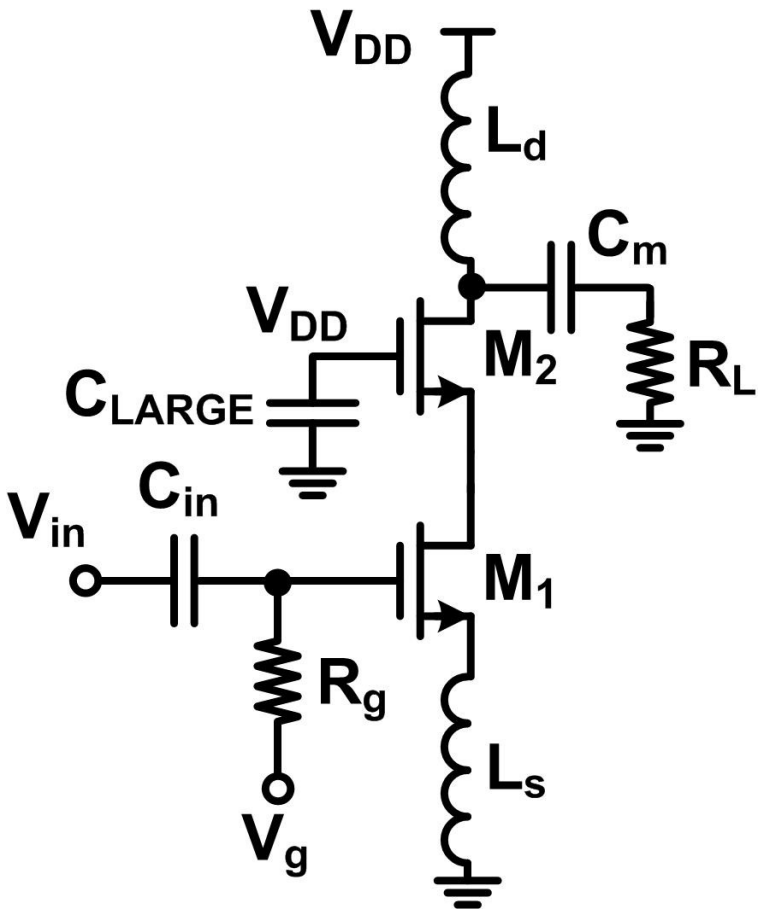




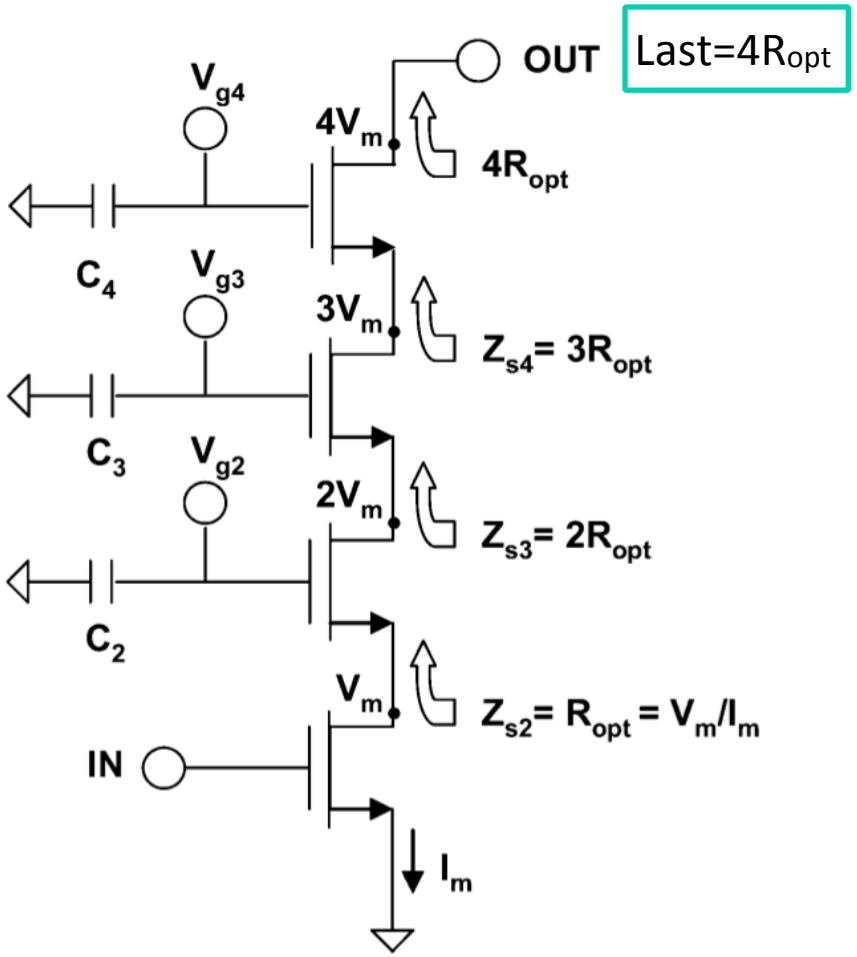
How to handle the high voltage?

Most common circuit solution:
the cascode
(stacked devices)

The voltage is however not evenly distributed between the transistors => not optimal (improved variants exist)



Transistor stacking: extending the concept



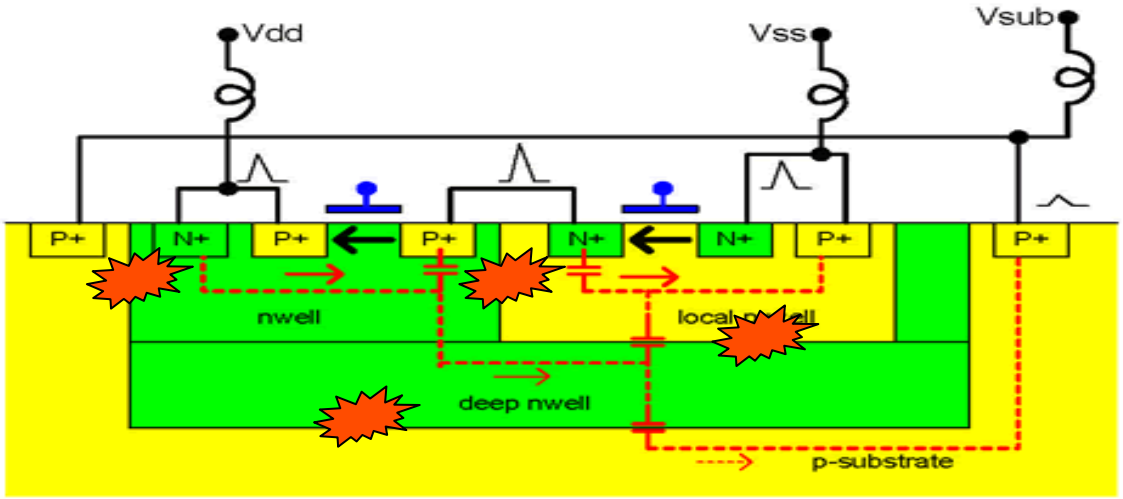
C_2, C_3, C_4 set Z_{s2}, Z_{s3}, Z_{s4}

$$Z_{\mathrm{si}} = \left(1 + \frac{C_{\mathrm{gs}}}{C_i}\right) \cdot \left(\frac{1}{g_m} \parallel \frac{1}{sC_{\mathrm{gs}}}\right)$$
$$\approx \left(1 + \frac{C_{\mathrm{gs}}}{C_i}\right) \cdot \frac{1}{g_m}, \qquad \text{for } f_0 \ll F_t.$$

In practice limited to four stacked devices

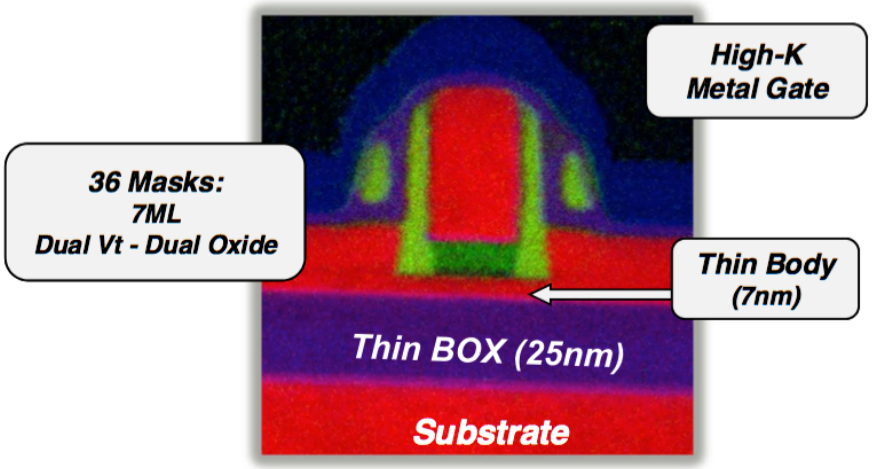
Chen et al., JSSC 2013

Limitation for maximum supply voltage

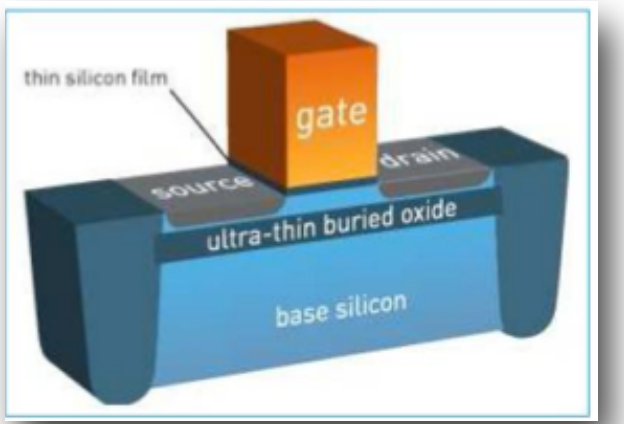


- Conventional bulk CMOS: many diode breakdowns to wells and substrate.
- Scaled bulk CMOS: breakdown voltages down to 4-5 V.
- Stacked bulk components (PA): will be limited by the drain-substrate breakdown of the uppermost transistor in the stack.
- With SOI, there is no breakdown to the substrate. Possible to stack components without breakdown voltage limitations.

28 nm FD-SOI (UTBB)



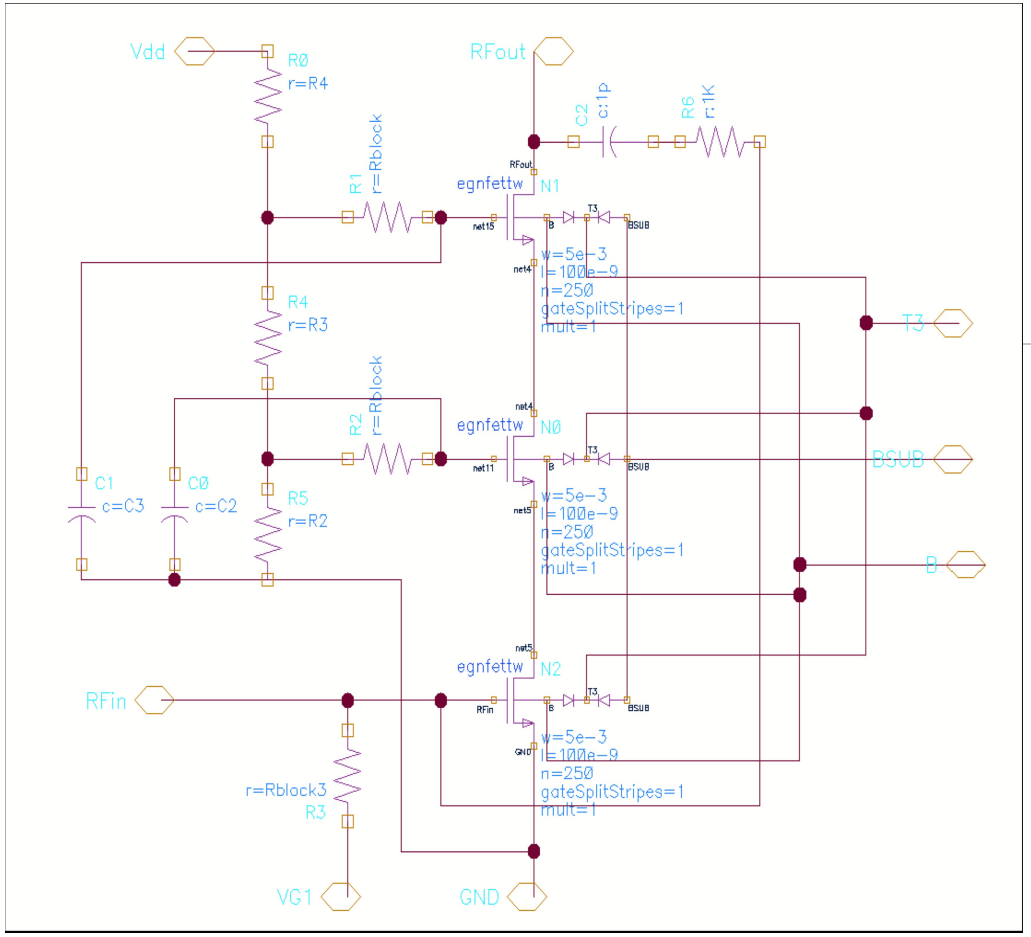
L_g=24 nm, T_{ox}=1.8 nm, V_{sup}=1.0 V
ultra-thin silicon: 7 nm
ultra-thin buried oxide: 25 nm



High-k dielectric
Metal-gate electrode
S/D: epitaxy raised
Undoped channel
Bulk/SOI integration

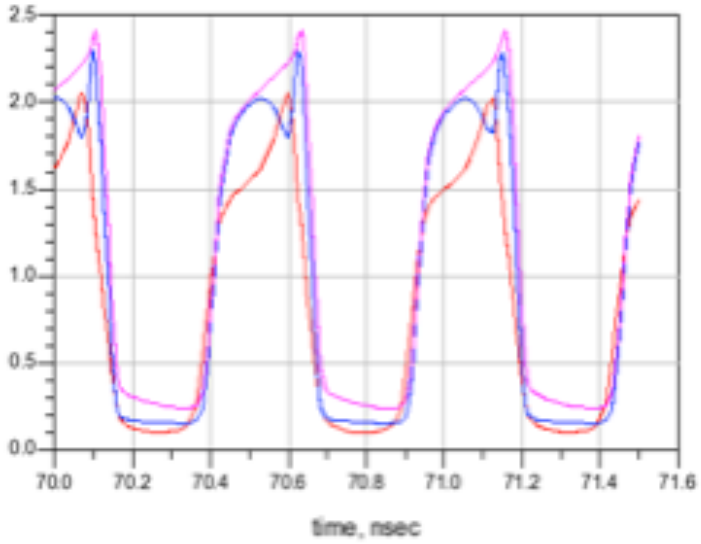
Stacked PA design:
L_g=150 nm, T_{ox}=2.8 nm,
V_{sup}=1.8 V (+10 %)

3-stacked high-power PA in 28 nm FD-SOI



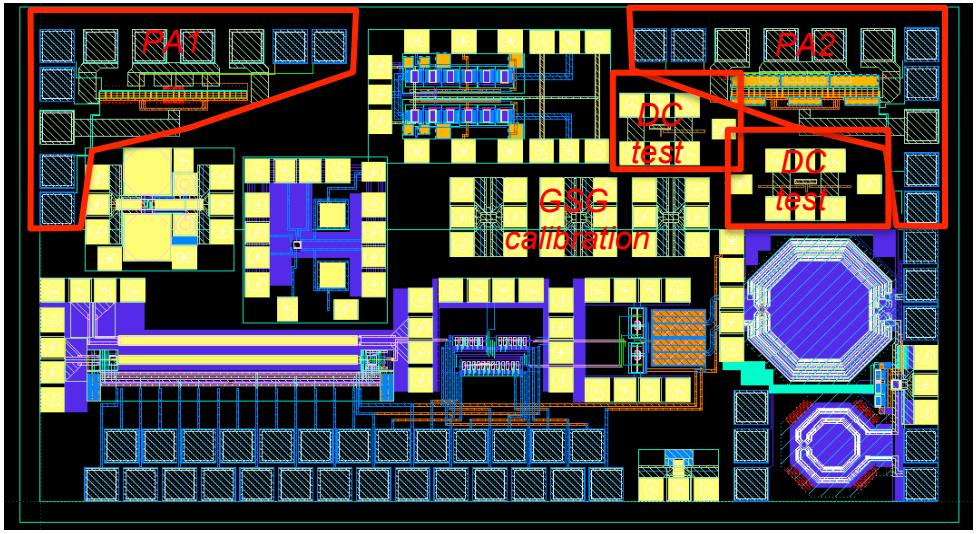
*W = 6000 um (10 um * 10 * 60 cells)*
Vdd=3.0 V
Class-AB
f=1900 MHz
*Zin = 0.49 + j*7.1 Ω*
RL=7 Ohm
C2=4 pF, C3=1 pF

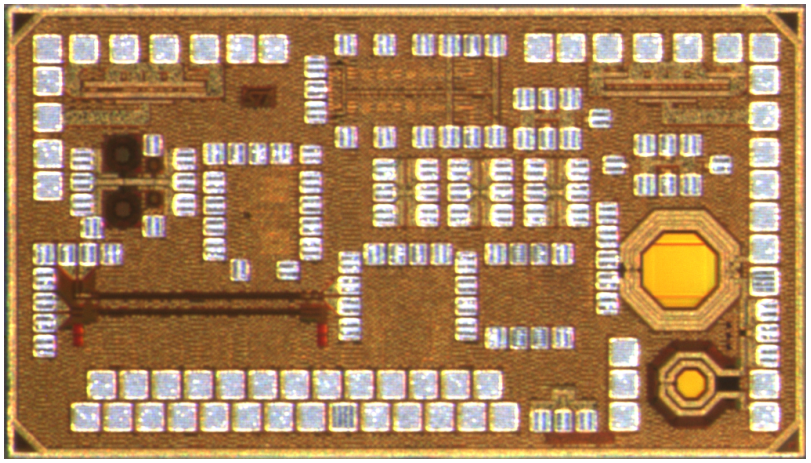
P-1dB= 28.9 dBm



3-stacked high-power PA in 28 nm FD-SOI

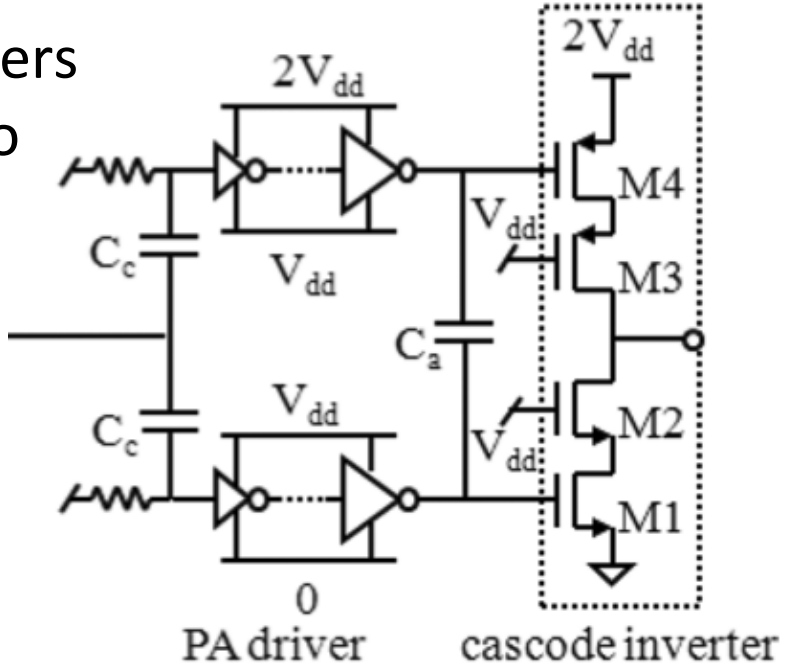
- Joint project Ericsson + Acreo Swedish ICT + LiU
- Area 1.5 x 2.2 mm
- Cost 50 k$
- Under evaluation





”Digital PA”

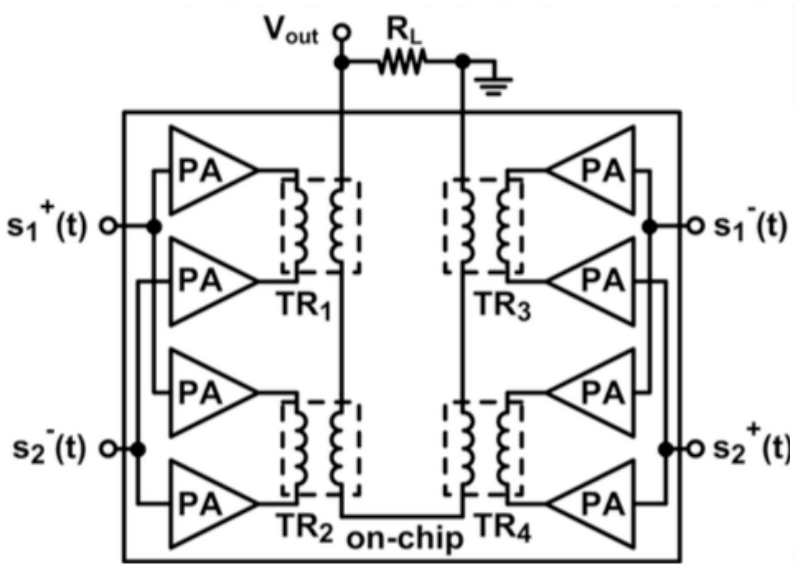
- CMOS-inverters can be used as switched PA, class D.
- They operate at normal (”digital”) supply voltage and has no over-voltage compared to other classes of PAs.
- In this particular case, the inverters are using a variant of cascode, so that the output stage can use 2 x V_{DD}, resulting in higher output power.

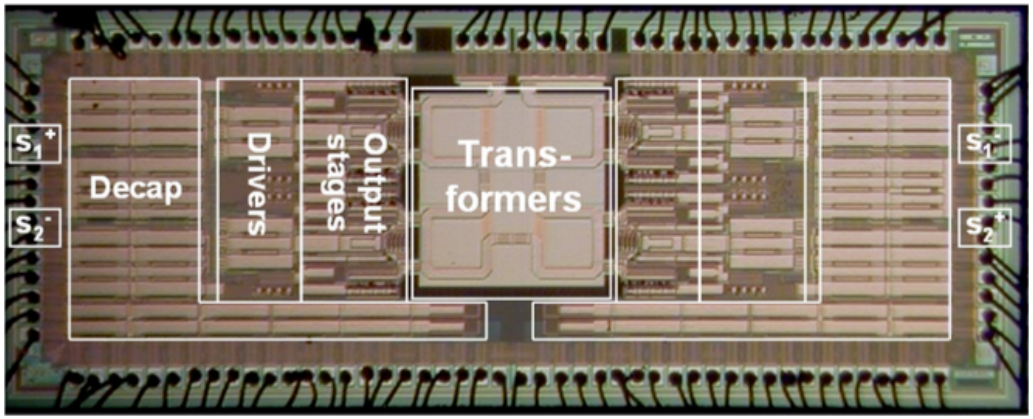


Xu et al., JSSC, 2011

”Digital PA” + transformer power combination

- The PAs are divided into 4 x differential PAs and power combined using an on-chip transformer.





4 x 1.5 mm, 130 nm CMOS

Fritzin et al., ESSCIRC 2011

Hot topic!

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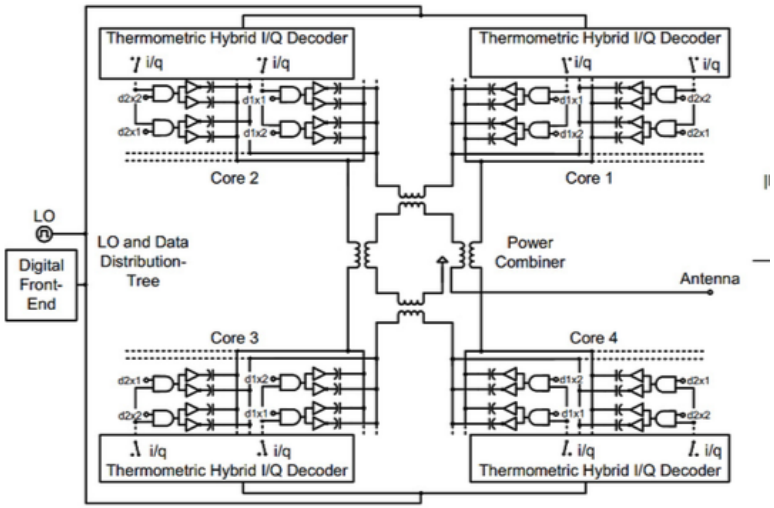
13.9 A 1.1V 28.6dBm Fully Integrated Digital Power Amplifier for Mobile and Wireless Applications in 28nm CMOS Technology with 35% PAE

Antonio Passamani[1], Davide Ponton[1], Edwin Thaller[1], Gerhard Knoblinger[1], Andrea Neviani[2], Andrea Bevilacqua[2]

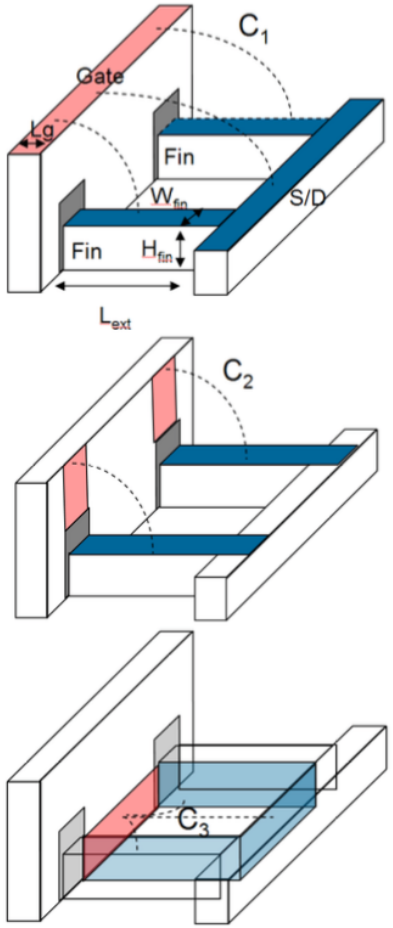
[1]Intel, Villach, Austria
[2]University of Padova, Padova, Italy



	This Work
Technology [nm]	28
Supply voltage [V]	1.1
Resolution [bit]	11
Carrier Freq. [GHz]	2.5
P_{sat} [dBm]	28.6
PAE @ P_{sat} [%]	35
Modulation signal	LTE 5-10MHz / WIFI 20-40MHz
P_{avg} [dBm]	20.7 / 17.3
EVM [%]	3.2-3.8 / 4.3-5.4
PAE @ P_{avg} [%]	14.6 / 11
ACLR [dBc]	-34.6/-44.7
w/ DPD	No
Area [mm^2]	1

FinFET and radio

- No recent examples in the literature of radio circuit demonstration using FinFETs (some at 45 nm node for pure research).
- Device simulation papers.
- Parasitic capacitances important!
- *”similar characteristics in terms of transconductance, Early voltage, voltage gain, self-heating issue but UTBB outperforms FinFET in terms of cutoff frequencies thanks to their relatively lower fringing parasitic capacitances.”* (Raskin, ”FinFET versus UTBB SOI - a RF perspective”, ESSDERC 2015)



Summary

- Moore and Dennard: continued transistor scaling, currently at 10 nm for large processors
- FinFET for RFIC design: lot of parasitics make radio design unfavorable.
- Integrated radio design: 28 nm CMOS (bulk or FD-SOI) is ”state-of-the-art”.
- A lot of tricks needed to reach high output power (>= 30 dBm or 1W), but possible and with good enough performance for popular applications.

Thank you for your attention!

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