Multi-standard challenges and solutions

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Outline

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The software defined radio

The vision is to have a generic hardware which can be programmed to any radio standard (compare the microprocessor)

Most initiatives from US military who want a single radio to cover all standards in use by all nations (33 “waveforms” from 2MHz to 2GHz). About 25B$ has been earmarked for JTRS (Joint Tactical Radio System)

Also great interest in civil market:
Single hardware gives very large cost reductions
Single radio in multistandard terminals:
GSM+3G+DECT/WLAN (UMA) for cell,
WLAN+WiMAX+EDGE+3G for laptop,
DVB-T+DVB-H+DAB for entertainment terminals
Managing non-stable standards, field upgradeability, multistandard handover
Frequency range 50MHz – 6GHz (except UWB, some WiMAX)
Radio challenges

Basic problems:

- **Weak signal from Tx in presence of strong disturber (blocker)**
  Requires very large dynamic range of frontend and channel filter with enough blocker suppression.

- **Signal from Tx may have several paths which interfere (variable when moving)**
  Requires advanced modulation / adaptive equalization / interleaving
  Very high demands on computation capacity (1-10 Pentiums)

Radio challenges

Antenna frontend  RF frontend  Digital baseband

Traditionally built on passive filters (LC-filters, SAW-filters) – not flexible

*How do we introduce frequency flexibility?*
Radio challenges

Fully programmable (or reconfigurable) antenna frontend
Same performance, no power penalty

Wide band RF frontend
Wideband or tunable LNA
Simplify by moving blocker problem to digital block
Higher performance ADC, no power penalty

Multiple band power amplifier
Highly linear, high efficiency

Fully programmable digital block
No silicon penalty, no power penalty

Lectures today:
Antenna frontend  Clemens Ruppel
RF frontend      Stefan Heinen
                Stefan Andersson
Power amplifier  John Gajadharsing
Digital baseband Dake Liu
Radio challenges

Weak signal from Tx in presence of strong disturber (blocker)

Example: blocker 1W, 1m distance, 10cm² effective antenna area: ~0.1mW (-10dBm)
Typical specs: In-band blocker -30dBm, out of band blocker -10dBm, 0dBm.

Two problems:
- Signal strength – too high signal may saturate amplifiers – weak signal blocked.
  Note: 0dBm in 50Ω gives 0.63V peak-to-peak, no room for gain!
- Intermodulation – 3rd order intermodulation gives intermodulation products at 
  $2f_1-f_2$ and $2f_2-f_1$, so if $f_1$ and $f_2$ is in the same band, the intermodulation product 
  is as well.
  We need very high linearity!

Multistandard challenges and solutions / Christer Svensson
**RF Frontend Challenge, based on simplification:**

channel filter in digital:

- 1W blocker 1m away: \( P_B = \frac{A_{\text{noise}}}{4\pi r^2} \) \( P_{\text{radio}} = m = -10\text{dBm} \)

Thermal noise density: \( S_i = F K T \) (F=9dB)

ADC noise density: \( S_A = \frac{V_i^2}{R_i} 2^{-2n} \frac{2}{f_s} = 2 \frac{2}{3} P B \frac{2^{-2n}}{f_s} \)

ADC requirements (\( S_A = S_i \)): \( f_s \frac{2^n}{3 F K T} = 4 \frac{P_B}{4 \cdot 10^5} = 4 \cdot 10^5 \)

**F**

\[
\text{Oversampling gains resolution}
\]

\[
\begin{array}{|c|c|c|}
\hline
f_s & \text{n} & \text{f_s} \\
\hline
5\text{GHz} & 10 & 9 \\
40\text{MHz} & 14 & 4 \\
\hline
\end{array}
\]

**Utilizing a 1st order \( \Sigma\Delta \)-loop in ADC**

Example: \( f_s = 20\text{MHz} \)

Further oversampling gain: \( \frac{3}{\pi^2} OSR^2 = \left( \frac{f_f}{2f_s} \right)^2 \)

\[
f_s \frac{2^n}{9} \frac{P_B}{F K T} f_s^2
\]
ADC perspective

Feasible solutions

- **Homodyne**, ADC $f_s=40$MHz, 14b Classical or sampling
- **Direct RF sampling**, multiple bit $\Sigma\Delta$ ADC $f_s=5$GHz CMOS
- **Direct RF sampling**, single bit $\Sigma\Delta$ ADC $f_s=40$GHz InP, SiGe (CMOS)

Note, linearity still 14b

ADC power consumption

Actual data from ISSCC 2002, 2006

Theory:
- Sampling power $P_s = 12kTf_s2^{2n}$
- Pipelined ADC $P \geq 80P_s$

(Svensson, Andersson and Bogner, Norchip 2006)
**Frequency planning**

Nyquist sampling: \( f_s \geq 2f_B \) - minimum sampling frequency

Nyquist sampling related to carrier: \( f_s \geq 2f_c \)

 Impossible filter

Nyquist sampling

0 \( \rightarrow \) \( f_c = f_s / 2 \) \( \rightarrow \) \( f_s \)

Simple filter

0 \( \rightarrow \) \( f_c = f_s / 4 \) \( \rightarrow \) \( f_s \)

2x Nyquist sampling

**Frequency planning**

Superheterodyne

0 \( \rightarrow \) \( f_{IF} \) \( \rightarrow \) \( f_{LO} \) \( \rightarrow \) \( f_c \) \( \rightarrow \) \( 2f_{LO} \)

Image frequencies

Zero IF

RF filter can not distinguish between carrier and image. By using a double mixer, producing I and Q, we may separate the carrier and image. (via local oscillator and a 90° Q signal)
Frequency planning

Sampling I/Q separation (equivalent to IQ mixer)

I-samples  Q-samples

RF

LO I

LO Q

Need LO’s with 90° phase difference
(digitally generated need 4f_c)

Sampling for digital I/Q separation

I-samples  Q-samples

RF

LO

T_{IF}

f_s = \frac{4f_{rf}}{2n-1}, n = 2
Frequency planning

Sampling for digital I/Q separation (I/Q-separation by sorting)

symmetric

0 \rightarrow f_c \rightarrow f_s \rightarrow 2f_s

f_s = f_c / 4, f_s = 3f_c / 4, f_c = 5f_s / 4, f_c = 7f_s / 4

Alternative carriers

(equivalent to 2x Nyquist sampling)

Flexible architectures

Minimum filter needs:

Homodyne with I/Q mixer/sampler

Filter = antialiasing only

Very high ADC sampling frequency, less filter
timediscrete – more robust

Channel filter in digital

Direct RF sampling

Very high sampling frequency

Digital bandpass filter at \( f_c \)
Flexible architectures

Homodyne with I/Q mixer
Common solution – often channel filter before ADC

Homodyne with sampler
Andersson, et. al. (2.4GHz/150MHz)

Timediscrete antialias filter
Mohammad, et. al.

I/Q sorting sampler
Jakonis, et. al. (1.07GHz/90MHz)

Timediscrete antialias filter

Homodyne
Blad, et. al. (2.4GHz/2.4GHz)

High $f_s$ $\Sigma\Delta$ converter

Direct RF sampling
Chalvatzis, et. al. (40GHz)

Very high $f_s$ bandpass $\Sigma\Delta$-converter

RF filter and LNA

Widely tunable filter
Electronically tunable LNA (active filter)
Multiple LC-filters (selection by MEMS switches?)

Low noise amplifier
Very large dynamic range – high linearity
Low noise figure
Wideband input impedance control

Blocker input -10dBm means 0.2V peak to peak – no room for gain!
Widely Tunable LNAs

Circuit topology, block diagram

a) Microwave recursive filter

b) CMOS recursive filter implementation

Widely Tunable LNAs

Tunable 0.75-3GHz
Recursive technique

Measured gain

Technology: 0.18µm CMOS
Size: 450x200µm² (excluding pads, no inductors),
900x900µm² (including pads)
Wideband LNA (0.13µm)

- Wideband common source amplifier
- 50Ω wideband matching by common drain feedback
- Negative capacitance compensates input capacitance
- Partly noise cancellation

Voltage Gain 17dB
Frequency range 1-7GHz
NF 2.4dB at 3GHz
IIP3 -4.1dBm
1-dB CP -20dBm
Power consumption (1.4V supply) 25mW
Active Area 0.019mm²
Radio challenges

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Signal from Tx may have several paths which interfere (variable when moving)

Different signal arrival times
Use subcarriers with very low bandwidth – OFDM (less sensitive to delays)
In DSS (CDMA), use rake receiver (several time-displaced detectors added)
Needs FFT’s and/or correlators

Channel distortion (dispersion, doppler shifts, time-variations)
Needs channel estimation + distortion compensation

Intermittent no signal due to interference
Needs interleaving (scrambling in time domain)

General quality improvements through forward error correction
Radio challenges

**Very high demands on computing capacity**

- 802.11a: 3 Pentiums, 30W
- UMTS: 10 Pentiums, 100W

Performance obtained with application specific hardware

Needs for programmability

Data from Kees van Berkel, et. al., Philips, SDR Technical Conference 2004

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Programmable baseband

Very promising results recently by DSP architectures specialized for baseband processing

Philips uses a combined SIMD/VLIW architecture
(vector processor + simple ALU controlled by long instruction words)

Stringent/Coresonic uses a Single Instruction stream, Multiple Tasks (SIMT) architecture
Conclusion

Software radio is a large challenge
Many elements of a solution are at hand
AD-converter performance can take care of full dynamic range
at acceptable power consumption
Programmable baseband processors has been demonstrated
Some areas still unresolved

References