On the Design of an Antenna Switch in 28 nm FD-SOI CMOS

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Introduction and Outline

• EU project within ECSEL
• Support ST Microelectronics with demonstrations of feasibility of FD-SOI
• Evaluations not yet finished

• 28 nm FD-SOI (UTBB)
• Antenna switch design and consideration
• Results from on-going work
UTBB vs. bulk CMOS
28 nm FD-SOI (STM)

$L_g=24$ nm, $T_{ox}=1.8$ nm, $V_{sup}=1.0$ V
ultra-thin silicon: 7 nm
ultra-thin buried oxide: 25 nm

High-k dielectric
Metal-gate electrode
S/D: epitaxy raised
Undoped channel
Bulk/SOI integration

"High-voltage" design:
$L_g=150$ nm, $T_{ox}=2.8$ nm,
$V_{sup}=1.8$ V (+10 %)
Limitations on the maximum voltage

- Conventional bulk CMOS: many possible diode breakdowns to well and substrate.
- Scaled bulk CMOS: breakdowns approaching 4-5 V.
- SOI: reduced problems with breakdown to the substrate, possible to stack components.
Design of RF-blocks on FD-SOI

- Broadband LNA
- Capacitive feedback LNA
- Passive double balanced resistive FET mixer
- LO distribution network
- PA core
- RF switch

Generic TDD radio front-end
Test chip = 1.5 x 2.2 mm$^2$
RF antenna switch (SPDT)

- 30 dBm
- 50 Ohm
- IL < 1 dB
- Isolation > 30 dB
- IM3 < -50 dBc
- f = 1.9 GHz
- 28 nm FD-SOI CMOS
Switch design in Cadence

- 30 dBm @ 50 Ohm => 10 $V_p$
- 6 stacked transistors (1.8 V + 10 %), W/L= 1 mm/150 nm
Pin = 30 dBm
By adding capacitors between the blocks, better phase balance was achieved.
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PCB design in ADS
Chip and testboard, ready for measurements

• Currently under evaluation
Problem with tie-down diodes

• Tie-down diode limits maximum power (voltage). Voltage peaks will cause diode to open to substrate.

• Test structure specific, not in integrated switch.
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