10.2 A *latch* holds its digital value during one of the clock phases. During the other clock phase, it is transparent and propagates to input to the output. There is never any transparency between the input and the output in the flip-flop.

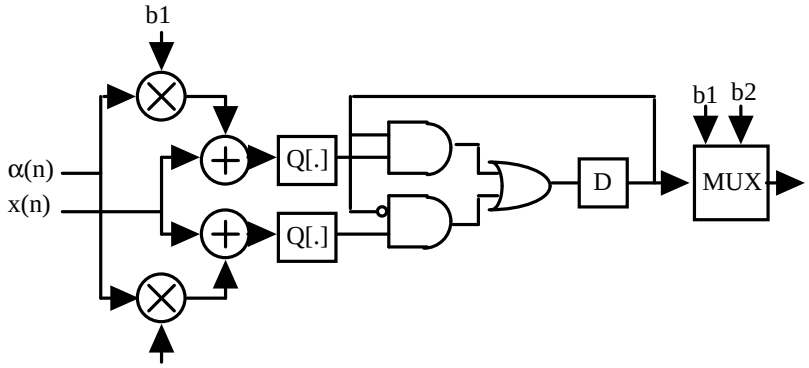
10.3 The flip-flop in Figure 10.12 has a positive feedback and does not need refresh. Hence this flip-flop is static. Obviously the outputs from both AND-gates are low when the clock is low, so the trigger edge for this flip-flop is the rising-edge of clock signal.

10.4 Circuits with logic style C^2MOS are examples for nonoverlapping two-phase clock implementation.

10.7 a) This type of quantization loop ocurr in for example: Differential pulse code modulation (DPCM), decision feedback equalizers (DFE), Vitterbi coders.

$$T_{min} = \frac{1}{T_{mult} + T_{add} + T_Q}$$

b)



New throughput is $T_{min} = \frac{1}{T_{and} + T_{or}}$