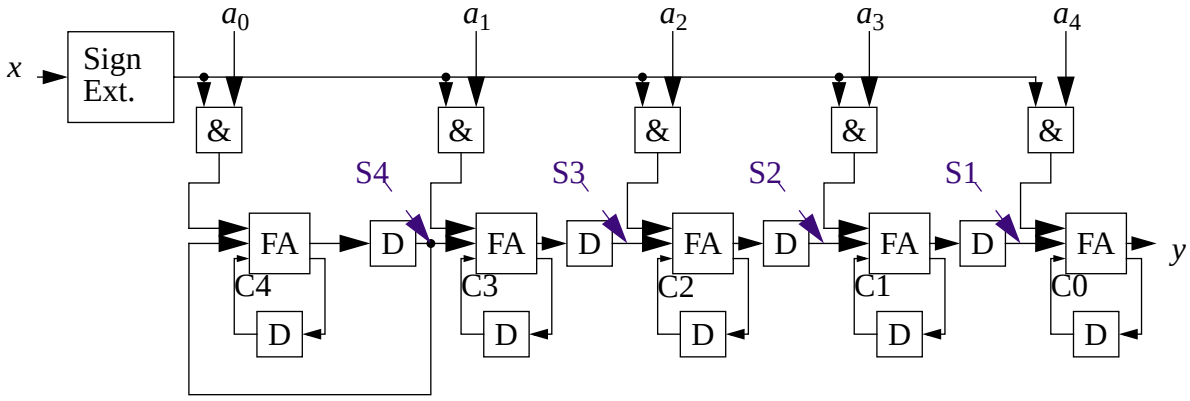
11.4 (a) $a = 1.1101$ and $x = 1.001$. The sign extension circuit extends the coefficient x to $W_d + W_c - 1 = 5 + 4 - 1 = 8$ bits, or, $x_{ext} = 11111.001$.

The multiplication with bit-serial multiplier is shown below.



Serial/parallel multiplier

	x	S4	S3	S2	S1	C4	C3	C2	C1	C0	y	
reset	0	0	0	0	0	0	0	0	0	0	0	(LSB)
x_{-3}	1	1	1	1	0	0	0	0	0	0	1	
x_{-2}	0	1	1	1	1	0	0	0	0	0	0	
x_{-1}	0	1	1	1	1	0	0	0	0	0	1	
x_0	1	0	0	0	1	1	1	1	0	1	0	
x_1	1	0	0	0	0	1	1	1	0	1	1	
x_2	1	0	0	0	0	1	1	1	0	1	0	
x_3	1	0	0	0	0	1	1	1	0	1	0	
x_4	1	0	0	0	0	1	1	1	0	1	0	(MSB)

The result is $0.00101010_2 = 0.1640625_{10}$.

$ax = (1.1101)_2 \cdot (1.001)_2 = (-0.1875)_{10} \cdot (-0.875)_{10} = (0.1640625)_{10}$.

(b) The S/P multiplier in figure 11.15 needs $(W_d + W_c - 1) + 1$ clock periods to process one data, so the throughput is $\frac{1}{(16 + 4 - 1) + 1} = \frac{1}{20}$ sample per clock period.

With S/P multiplier in Figure 11.45, the throughput is doubled, i.e., $\frac{1}{10}$ sample per clock period.