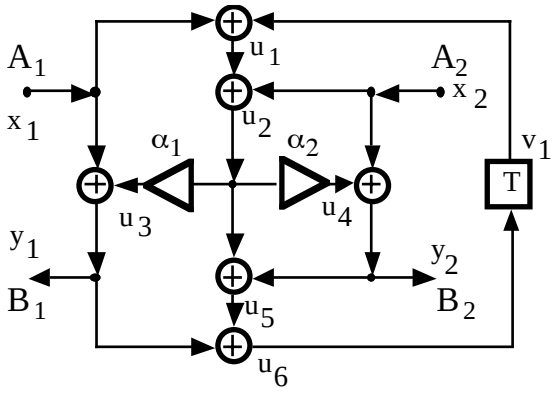
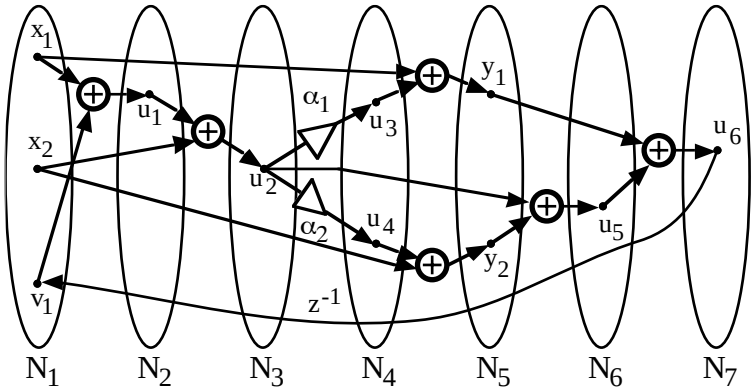
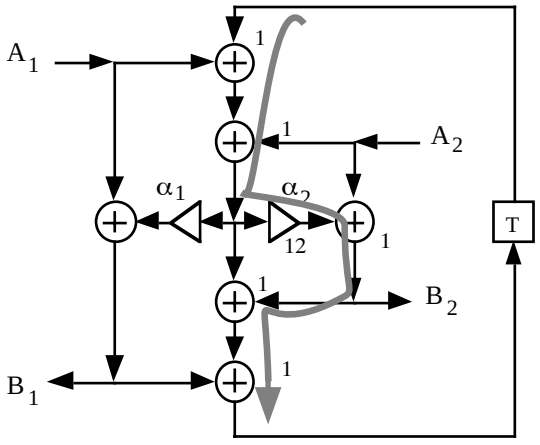
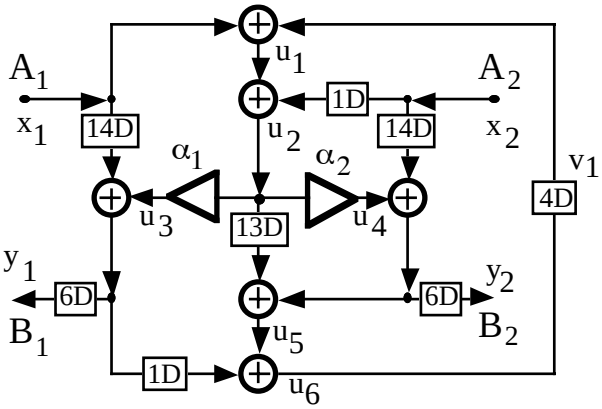
6.14 a) The first step is to convert the signal-flow graph into a fully specified SFG, since it contains two three-input adders. The resulting SFG is shown to the right and the resulting precedence graph is shown below.




b) The critical path is $v_1 u_1 u_2 u_4 y_2 u_5 u_6$

The length of this path is 1+1+12+1+1+1 = 17 clock cycles.

The maximal sampling rate is $f_{max} = 1/T_{min} = 60\ 10^6/17 = 3.5$ MHz

c)The adaptor with shimming delays is shown to the right above.