8.2 The main limitation in shared memory architectures is the memory bandwidth bottleneck, i.e., the PEs have to wait for the access of data, which stored in the shared memory. There are serveral methods to overcome this limitation: reducing the memory cycle time, reducing communications from PEs to memory, increasing the execution time for the PEs. The reduction of the memory is the most straightforward solution and the implementation are often based on using more small memories in stead of a large memory. The main drawback in this solution is the overhead for the rearrangement of data. The reduction the communications is using the DSP algorithm to reduce the access to the memory. The methods which are discussed in section 8.9.3 depends highly on the algorithm which cannot “transfer” from one algorithm to another. The increasing the execution time for the PEs is either increase the basic operations or slower the PEs. These solutions depends on both the DSP algorithm and the performance requirement. In generally, we have to study the design specificationcarefully and select the balanced architecture in order to achieve a more optimal solution. (See also section 8.9).