8.1 An ideal archietecture has processing elements that can execute the operations according to the schedule and is supported with appropriate communication channels and memories. The criteria for ideal architecture are: predictable schedule that fullfil the target applications; proper processors, memories and communications that perform the schedule.

8.2 The main limitation in shared memory architectures is the memory bandwidth bottleneck, i.e., the PEs have to wait for the access of data, which stored in the shared memory. There are serveral methods to overcome this limitation: reducing the memory cycle time, reducing communications from PEs to memory, increasing the execution time for the PEs. The reduction of the memory is the most straightforward solution and the implementation are often based on using more small memories in stead of a large memory. The main drawback in this solution is the overhead for the rearrangement of data. The reduction the communications is using the DSP algorithm to reduce the access to the memory. The methods which are discussed in section 8.9.3 depends highly on the algorithm which cannot “transfer” from one algorithm to another. The increasing the execution time for the PEs is either increase the basic operations or slower the PEs. These solutions depends on both the DSP algorithm and the performance requirement. In generally, we have to study the design specificationcarefully and select the balanced architecture in order to achieve a more optimal solution. (See also section 8.9).

8.3 Peak throughput:

$$16 \text{ PEs} \cdot 2 \text{ op} \cdot 125\ 10^6 = 4\ 10^9 \text{ oper./s} = 4 \text{ GOPS}$$

I/O:

$$2 \text{ channels} \cdot 4 \text{ sides} \cdot 125\ 10^6/(2 \text{ cycles}) \cdot 12 \text{ bits} = 6 \text{ Gbits/s} = 750 \text{ Mbytes/s}$$

8.4 There are various standard DSP processors. Here are a few examples(1999):

- Texas Instruments TMS320C67xx, TMS320C27xx...
- Analog Devices ADSP-2116x...
- ARM ARM7TDMI...
- ZSP ZSP164xx...
- Lucent Technologies DSP16xxx...
- LSI Logic LSI401Z...
- Motorola DSP 560xx, DSP 563xx, DSP 568xx...
- IBM C54XDSP...
- ...

Check the relative companies’ web sites for curent information.

8.6 Assume that the area scales quadratically which is somewhat pesimistic since the number of metal layers are increased in modern processes. TMS320C25 is manufactured in a 1.8 μm CMOS technology and with a clock frequency of 50 MHz. If the 0.35 μm technology is used, the area can be reduced to $\frac{(0.35)^2}{(1.8)^2} = 0.04$, or to about 4% of the original area.

The clock frequency can be estimated according to equation (2.6). The 1.8 μm process has a threshold voltage in the range 0.8~0.9V and the 0.35 μm has a threshold

voltage in the range 0.5~0.6V. We take $V_{T_{1.8\mu m}} = 0.8\,\text{V}$ and $V_{T_{0.35\mu m}} = 0.5\,\text{V}$, the maximum clock frequency can be estimated by

$$f_{0.35\mu m} \approx \frac{(V_{DD_{0.35\mu m}} - V_{T_{0.35\mu m}})^{1.55}}{(V_{DD_{1.8\mu m}} - V_{T_{1.8\mu m}})^{1.55}} \cdot \frac{V_{DD_{1.8\mu m}}}{V_{DD_{0.35\mu m}}} \frac{C_{L_{1.8\mu m}}}{C_{L_{0.35\mu m}}} \cdot f_{1.8\mu m}$$

$$\approx \frac{(3.3 - 0.5)^{1.55}}{(5 - 0.8)^{1.55}} \cdot \frac{5}{3.3} \cdot \left(\frac{1.8}{0.35}\right)^2 \cdot 50 \times 10^6 \approx 1 \times 10^9 (\text{Hz})$$

However, there are many other problems in designing such high frequency processors, like clock skew and power supply, etc. The most DSP processor are running at 100 MHz to 200 MHz currently while general purpose processors are running at 500 to 800 MHz.

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