9.20 The delay time and supply voltage is given by

$$t = \frac{C_{load} V_{supply}}{k(V_{supply} - V_T)^2} \quad (1)$$

where k is a factor depends on the technology and size of transistors and it is a constant for voltage scaling, the same for C_{load}.

The power consumption is given by

$$P = C_{load} V_{supply}^2 f_{clk} \quad (2)$$

The sample rate is 10 MHz corresponds to a clock frequency of 30 MHz.

$$T_{clk} = \frac{1}{30 \times 10^6} s = 33.3 ns$$

Compare it with the case of 35 MHz, or clock frequency of 105 MHz

$$T_{oldclk} = \frac{1}{105 \times 10^6} s = 9.52 ns$$

From equation (1), we can scale down the voltage from 5 V to 2.24 V, so the power consumption can be reduced to

$P_{new} = \frac{2.24^2 \times 30 \times 10^6}{5^2 \times 105 \times 10^6} \cdot P_{old} = 0.0572 \times 30 mW = 1.72 mW$ according to equation (2).