Syed Asad Alam

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OBJECTIVE

Conduct research on the design and implementation of signal processing and communication algorithms on FPGAs/ASICs

SUMMARY

- Around 4 years experience in design, implementation and verification of FPGA based signal processing and communication systems.
- **Expertise:** FPGA based system design using Verilog HDL, VHDL and System Verilog.
- **Tools:** ModelSim, NanoSim, Design Analyzer, Xilinx ISE, Altera Quartus I/II, FPGA Advantage, Cadence Virtuoso, Matlab, Simulink, Altera DSP Builder, Gurobi Optimizer
- **Languages:** Verilog HDL, VHDL, System Verilog, C, Python

ACADEMIC INFORMATION

Linköping University, Linköping, Sweden **2010 – Present**
PhD Student, Division of Electronics Systems, ISY

Linköping University, Linköping, Sweden **2008 – 2010**
M.Sc.EE with specialization in System on Chip Design

N.E.D. University of Engineering and Technology **2003 – 2007**
B.E. in Computer and Information Systems Engineering

PHD RESEARCH AREA

The focus of research is on the efficient implementation of different algorithms using in signal processing and digital communication on FPGAs and ASICs.

PUBLICATIONS

- S. A. Alam and O. Gustafsson, "Implementation of time-multiplexed sparse periodic FIR filters for FRM on FPGAs," in *Proc. IEEE Int. Symp. Circuits Syst.,* Rio de Janeiro, Brazil May 2011
- S. A. Alam and O. Gustafsson, " Implementation of narrow-band frequency-response masking for efficient narrow transition band FIR filters on FPGAs," in *Proc. Norchip,* Lund, Sweden, Nov. 2011

MASTER'S THESIS

DESIGN SPACE EXPLORATION OF FIR FILTERS ON FPGAS

Thesis work revolved around exploring implementation of Time Multiplexed Architectures on FPGAs and comparing their performance against FIR Cores available from Xilinx. Specifically two architectures were explored, Linear and Non-Linear Phase FIR Filters. Results of interest were logic slice count, operating frequency, scaling, power consumption, word length effects and comparison against Xilinx FIR core.

Report – Presentation

Academic Projects

- **Design of PHY Layer of 802.11a WLAN (System Design)**
  Role: Team Lead Team Size: 5 Duration: 4 months
  Report – Presentation
- **DLL based Frequency Multiplier (VLSI Design)**
  Role: Team Lead Team Size: 5 Duration: 5 months
  Report – Presentation
- **Design of a High Speed, Low Power 16x16 Multiplier (Low Power Electronics)**
  Team Size: 2 Duration: 2 months
  Report
- **Echo Generation on DE2 Board using VHDL (Design of Digital Systems)**
  Role: Team Member Team Size: 6 Duration: 2 months
  Report – Presentation
- **Design and Implementation of SIMD DSP (B.E. Final Year Project)**
  Report – Presentation

Teaching Experience

Teaching Assistant – ASIC for DSP(TSTE87), Design of Digital Systems(TSTE12), Digital Arithmetic(TSTE18)
2010 – Present

Teaching Assistant - Digital Integrated Circuits(TSTE86)
August 2010 – October 2010

Lab Assistant – Low Power Electronics(TSTE85)
October 2009 – December 2009

Work Experience

PhD Student – Dr. Oscar Gustafsson, Division of Electronic Systems, Department of Electrical Engineering, Linköping University (www.es.isy.liu.se)
March 2010 – Present

Research Assistant – Dr. Oscar Gustafsson, Division of Electronic Systems, Department of Electrical Engineering, Linköping University (www.es.isy.liu.se)
January 2010 – March 2010

Hardware Design Engineer – Digitek Engineering (www.digitekeng.com)
June 11, 2007 – August 18, 2008

Had been part of the following projects
Pseudo Wire Emulation Edge-to-Edge, CIC and CFIR Filter for DDC and DUC, 10G Pattern Matching Solution, T1/E1 Line Interface

VLSI Design Engineer - SSUET Research Center
Feb 2, 2006 –Sep 30, 2006

References

- Oscar Gustafsson – Associate Professor and Head of Electronics Systems Division, Department of Electrical Engineering, Linkoping University, Sweden – oscarg@isy.liu.se
- Fasahat Hussain – Senior Technical Manager, Digitek Engineering, Karachi, Pakistan – fasahat@digitekeng.com